FUJI Power Supply Control IC

Power Factor Correction

FA5612 / FA5613

Application Note

'11-4

Fuji Electric Co.,Ltd.

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   - Communications equipment (terminal devices)
   - Measurement equipment
   - Machine tools ·Audiovisual equipment
   - Electrical home appliance
   - Personal equipment
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   - Emergency equipment for responding to disasters and anti-burglary devices
   - Safety devices

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   - Aeronautic equipment
   - Atomic control equipment
   - Submarine repeater equipment
   - Medical equipment

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Note

- The contents are subject to change without notice for specification changes or other reasons.
- Parts tolerance and characteristics are not defined in all application described in this Date book. When design an actual circuit for a product, you must determine parts tolerance and characteristics for safe and economical operation.

1. Description

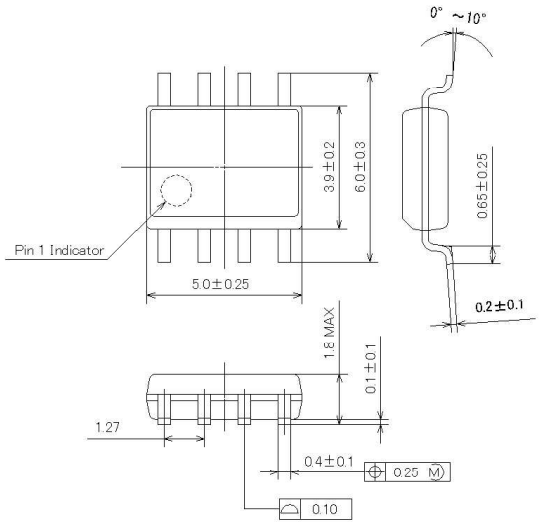
FA5612/13 is control IC for power factor correction converter. It realizes low power consumption by using high voltage CMOS process. Thanks to a average current control, a stable operation is obtained, whereby a power factor of 99% or more is easily available. DC output voltage is controlled under a wide range of load from rated to no load. Further, a unique switching frequency diffusion function incorporated simplifies the line filter.

2. Features

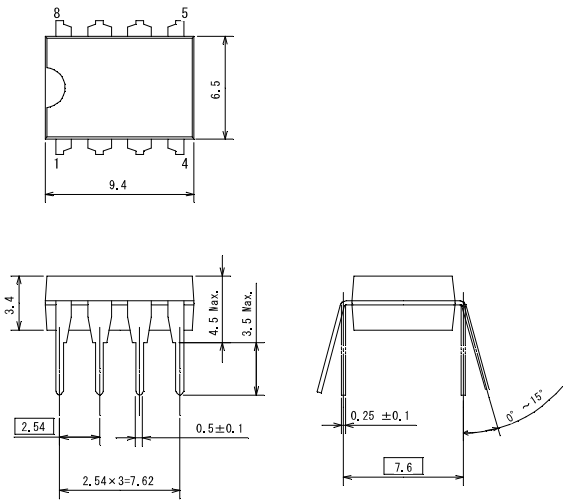
- Unique switching frequency diffusion function incorporated
- Selectable switching frequency : Diffuse or Fix (60 kHz, 65 kHz)
- High-precision over current protection : 0.5V ± 5%
- No audible noise at startup by dynamic OVP circuit
- Low current consumption by high voltage CMOS process
  Operating : 2mA (typ.)
- Enabled to drive power MOSFET directly.
  Output peak current, source : 1.5A, sink : 1.5A.
- Open/short protection at feedback (FB) pin
- Under-voltage lockout
  FA5612 : 9.6V ON / 9V OFF FA5613 : 13V ON / 9V OFF
- 8-pin package: SOP-8, DIP-8

3. Outline

SOP-8



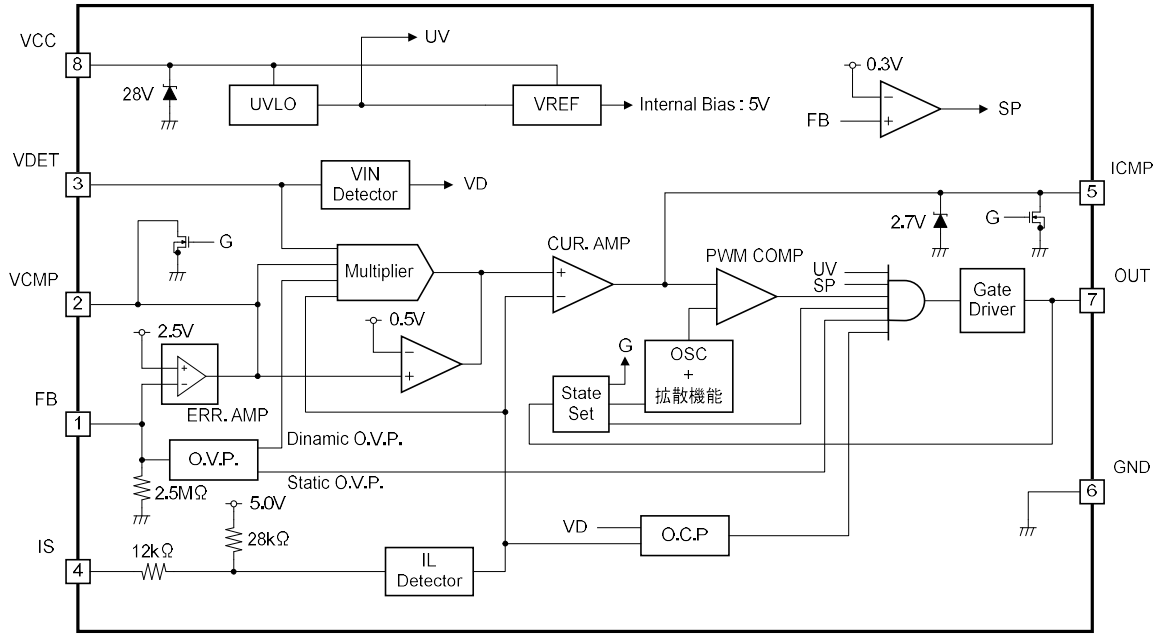
DIP-8



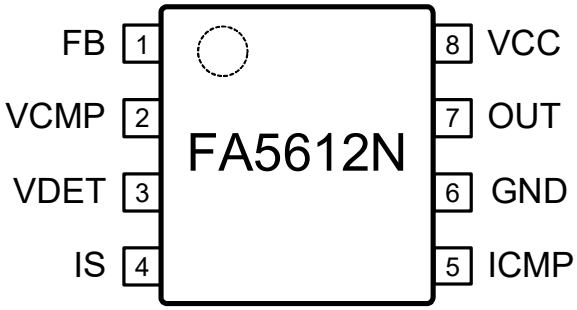
4. Type of FA5612/13

Type	Startup Threshold	Package
FA5612N	9.6V (typ.)	SOP-8
FA5612P	9.6V (typ.)	DIP-8
FA5613N	13V (typ.)	SOP-8

5. Block diagram



6. Pin assignment



Pin No.	Pin symbol	Function	Description
1	FB	Voltage Feedback Input	Inverting input for voltage error amplifier. Input terminal of converter output voltage.
2	VCMP	Voltage Loop Compensation	Output of voltage error amplifier. Phase compensator circuit is connected. *2
3	VDET	AC Voltage Input	Input terminal for sinusoidal AC input voltage waveform.
4	IS	Current Sense Input	Input terminal for inductor current signal.
5	ICMP	Current Loop Compensation	Output of current error amplifier. Phase compensator circuit is connected. *2
6	GND	Ground	Ground
7	OUT	Output	Output for driving a power MOSFET.
8	VCC	Power Supply	Power supply for IC control circuit and output circuit. *1

*1 connect the capacitor.
*2 connect capacitor and the resistor.

7. Ratings and characteristics

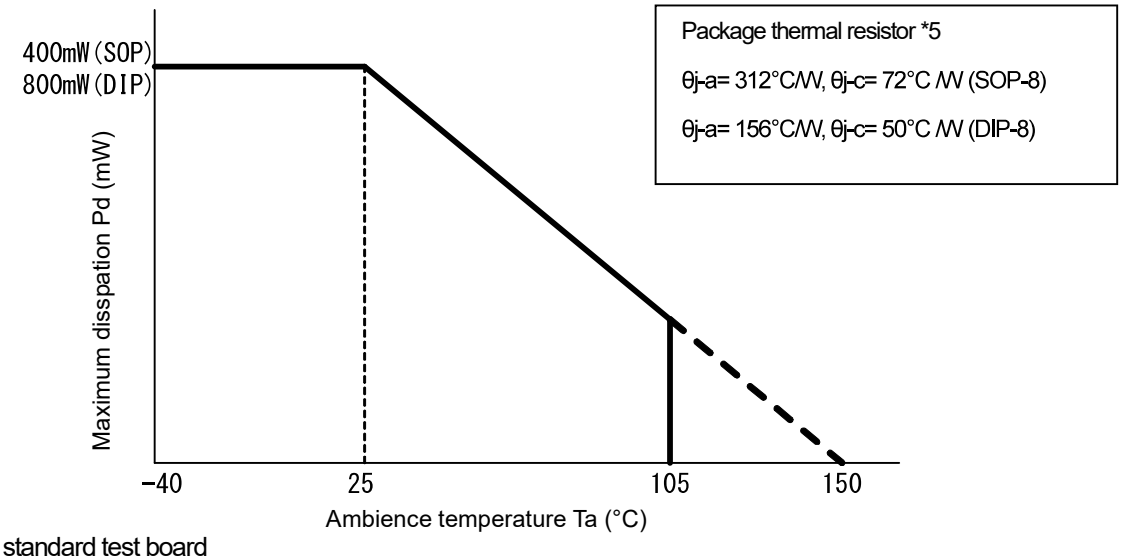
The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.
Stress exceeding absolute maximum ratings may malfunction or damage the device.
"+" shows sink and "–" shows source in current prescription.

(1) Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Total power supply and Zener Current (VCC) *1		Icc+Iz	15	mA
Supply Voltage (VCC) *1	Icc > 4.8mA	Vcc1	- 0.3 to 28	V
	Icc < 4.8mA	Vcc2	- 0.3 to Self Limiting	V
Output voltage (OUT) *4		Vout	- 0.3 to VCC + 0.3	V
Output current (OUT) *1		Iout	- 1500 to 1500	mA
Output peak current (OUT) *2		Iout_pk	Self Limiting	mA
input voltage (FB , VDET)		Vfb,Vvdet	- 0.3 to 5.0	V
Input current (FB , VDET) *3		Ifb,Ivdet	-100 to 100	µA
Input voltage (VCMP)		Vvcmp	- 0.3 to 5.0	V
Input current (VCMP) *3		Ivcmp	- 0.5 to 30	mA
Input voltage (ICMP)		Vvcmp	- 0.3 to 5.0	V
Input current (ICMP) *3		Iicmp	- 0.2 to 30	mA
Input voltage (IS)		Vis	- 5.0 to 1.0	V
Input current (IS) *3		Iis	- 300 to 100	µA
Power dissipation	DIP-8	Pd1	800	mW
	SOP-8	Pd2	400	mW
Operating Junction Temperature		Tj	- 30 to +150	°C
Storage temperature		Tstg	- 40 to +150	°C

*1 Must not exceed power dissipation.
*2 Period exceeding 1500mA must be 100ns or less.
*3 When the pin current flows continuously for 100ns or more.
*4 The period of 100ns (dead time period) when the voltage of the terminal OUT changes Low⇒High is out of the question.

Maximum dissipation curve



*5 JEDEC standard test board

(2) Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	10	18	26	V
VDET pin input voltage	Vvdet	0	-	2.4	V
VDET pin peak input voltage	Vpvdet	0.54	-	2.4	V
IS pin voltage	Vis	- 1.0	-	0.5	V
IS pin connection noise filter resistance	Risf	-	-	100	Ω
Ambiance temperature in operation	Ta	-40	-	105	℃

Item		Symbol	Resistance	Accuracy	Temperature characteristics
Frequency setting resistance *2	Frequency diffusion	Rg1	4.7kΩ	±5%	200ppm/°C
	65kHz fixed	Rg2	12kΩ	±2%	200ppm/°C
			13kΩ	±5%	200ppm/°C
	60kHz fixed	Rg3	27kΩ	±5%	200ppm/°C

*2) For connection in Fig.2, Ro range: 0 to 100Ω

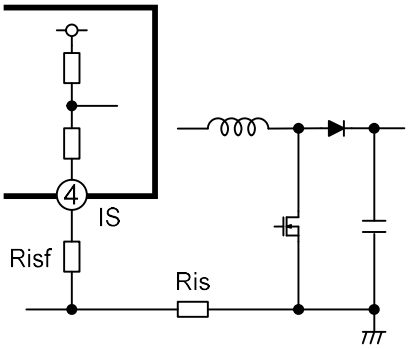


Fig.1 IS pin-connected filter resistance

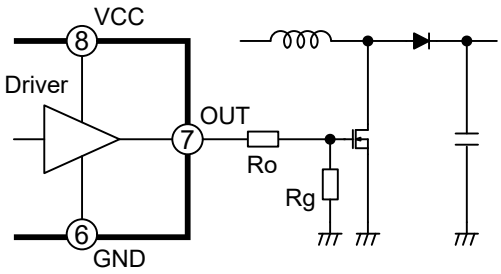


Fig.2 Frequency setting resistance

(3) Electrical Characteristics (Unless otherwise specified, Vfb=2.5V, Vvcmp=2.5V, Vvdet=0V, Vis=0V, Vicmp=2.0V, Vcc=18V, Rg=4.7kΩ, Tj=25°C)

"+" shows sink and "–" shows source in current prescription.

Voltage amplifier (FB, VCMP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage feedback input threshold	Vref	Ivcmp = 0uA	2.450	2.500	2.550	V
Line regulation	Regline	Vfb = Vref, Vcc = 10V to 26V	- 12.5	-	12.5	mV
Temperature stability	VrefdT	Vfb = vref, Tj = - 30°C to 150°C	- 0.5	-	0.5	mV/°C
Transconductance	Gmv	Vfb = Vref ± 0.3V	70	90	120	µmho
VCMP output current	Ivsrc	Source : Vfb = 1.5V	- 70	- 50	- 30	µA
	Ivsnk	Sink : Vfb = 3.5V	30	50	70	µA
VCMP output H voltage	Vvcmph	Vfb = 1.5V	-	-	5.5	V
VCMP transient response output current	Iresp	Source : Vfb = 1.5V	- 170	- 140	- 110	µA
VCMP transient response detection voltage	Vresp		0.902 *Vref	0.940 *Vref	0.978 *Vref	V

Current amplifier (ICMP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transconductance	Gmc	Vis= - 0.2V to - 0.4V, Vvdet *1	40	60	80	µmho
Output current	Icsrc	Source : Vvdet = 3.5V	- 70	- 50	- 30	µA
	Icsnk	Sink : Vis = -2.0V,	30	50	70	µA
ICMP clamp voltage	Vclamp	Vicmp = 3.0V Iicmp max = 320µA	2.6	2.7	2.9	V

*1 Vvdet is for when Vis = -0.3V, Iicmp = 0µA

Multiplier

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VDET input bias current	Ivdet	Vvdet = 0V,	- 1.5	-0.5	0	µA
VCMP threshold voltage	Vthvcmp	Vvdet = 2.4V	0.3	0.5	0.7	V
Output voltage coefficient	K	Vvcmp = 1V, Iicmp = 0µA Vvdet = 0.3V, 1.3V Vis = 0.1V to -0.2V	0.5	0.70	0.95	-

Oscillator

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency diffusion (reference frequency)	Fswref	Vvdet = 0.88V, Vis = - 0.18V, Vvcmp *1, Iicmp = 0µA,	54	60	66	kHz
Frequency temperature stability	FswrefdT	Vvdet = 0.88V, Vis = - 0.18V, Vvcmp *1, Iicmp = 0µA,Tj=-30°C to 125°C	-0.06	-	0.06	kHz/°C
Frequency diffusion (maximum frequency)	Fswmax	Vvcmp = 0V, Vvdet = 2.4V	64	68	70	kHz
Frequency diffusion, (minimum frequency)	Fswmin	Vvcmp = 0V, Vvdet = 0V	50	52	55	kHz
Fixed frequency 1	Fsw1	Vout2 < Vout	54	60	66	kHz
Fixed frequency 2	Fsw2	Vout1 < Vout < Vout2	58.5	65	71.5	kHz
Maximum duty cycle	DMAX	Vvdet = 2.4V, ICMP no connect	91	94	97	%

*1 Vvcmp is for when Vvdet = 0.88V, Vis = -0.18V, Iicmp = 0µA

Overvoltage protection comparator (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Static OVP threshold voltage	Vsovp	Vfb = 2.5V to 2.9V, Vvcmp = 0V, Vvdet = 0V	1.070*Vref	1.090*Vref	1.105*Vref	V
Hysteresis	Vsovphys	Vfb = 2.9V to 2.5V, Vvcmp = 0V, Vvdet = 0V	0.005*Vref	0.020*Vref	0.040*Vref	V
Static OVP temperature stability	VsovpdT	Vfb = 2.5V to 2.9V, Vvcmp = 0V Vvdet = 0V, Tj= -30°C to 125°C	-0.0001*Vref	-	0.0001*Vref	V/°C
Dynamic OVP threshold voltage	Vdovp	Vfb = 2.5V to 2.8V, Vvcmp = 1V, Vvdet = 2V	1.025*Vref	1.050*Vref	1.075*Vref	V
⊿OVP	⊿OVP	Vsovpn -Vdovp	50	95	140	mV

FB short detection comparator (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input threshold voltage	Vthfb	Vfb = 0V to 1V, Vvcmp = 0V	0.1	0.3	0.5	V
Pull-down resistance	Rfb	Vfb = 2.5V	2.0	2.5	3.0	MΩ

Overcurrent detection comparator (IS pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IS offset voltage	Visof	Vvdet = -0.25V, Vvcmp = 0.6V	0	30	60	mV
IS pin voltage	Vis_054	Vvdet = 0.54V, Vvcmp = 5.0V	- 0.43	- 0.38	- 0.33	V
IS threshold voltage	Vocpl	Vvdet max = 1.2V, Vvdet min = 0V, Fvdet = 50kHz, Dvdet=50%	- 0.525	- 0.50	- 0.475	V
	Vocph	Vvdet max = 1.8V, Vvdet min = 0V, Fvdet = 50kHz, Dvdet=50%	- 0.432	- 0.40	- 0.368	V
IS threshold voltage temperature characteristics	VocpldT	Vvdet max = 1.2V, Vvdet min = 0V, Fvdet = 50kHz Dvdet=50%,Vis = -0.4V to -0.6V Tj=-30°C to 125°C	- 0.1	-	0.1	mV/°C
VDET threshold voltage	Vvdeth	Vvdet max = 1.2V, to 1.8V Vvdet min = 0V, Fvdet = 50kHz Dvdet=50%,Vis= -Vocpl + 0.05V	1.54	1.60	1.66	V
	Vvdetl	Vvdet max = 1.8V to 1.0V, Vvdet min = 0V, Fvdet = 50kHz Dvdet=50%,Vis= -Vocpl + 0.05V	1.30	1.35	1.40	V
IS threshold change voltage	Vvdets	Vvdet max = 1.8V Vvdet min = 0V, Fvdet = 50kHz Dvdet=50%,Vis= -Vocpl + 0.05V	0.25	0.30	0.35	V
Blanking time *1	Tblk	Vis= -0.6V	300	450	600	ns
Delay time	Tdly	Vis = Vocpl + 30mV to-1.0V Pulse signal	200	350	500	ns
Input bias current	Iis	Vvcmp = 0V, Vis = 0V	- 170	- 120	- 70	µA

*1 Includes delay time

Output (OUT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage (L)	Voutl	Vfb = 0V, Vvcmp = 0.3V, Vicmp = 3V to 2V, Sink : Iout = 100mA	-	0.5	1.0	V
Output voltage (H)	Vouth	Vvcmp = 0.3V, Vicmp = 3V to 2V, Source : Iout = - 100mA	15.5	16.5	-	V
Output rise time	Tr	C_L = 1nF	-	50	-	ns
Output fall time	Tf	C_L= 1nF	-	50	-	ns

Frequency setting (OUT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection current	Istate	Tj=-30°C to 125°C	34	40	46	µA
OUT threshold voltage	Vout1	Tj=-30°C to 125°C	260	310	390	mV
	Vout2	Tj=-30°C to 125°C	700	760	830	mV
Frequency setting time *1	Tset	Vvcmp = 0V, Vicmp = 0V Vfb = 2V	4.1	5.9	7.7	ms
Detection time *2	Tdet	Vvcmp = 0V, Vicmp = 0V VFfb= 2V	420	530	640	µs

*1: Time elapsing until detection current is outputted from OUT pin after removal of UVLO
*2: Period during which detection current is outputted from OUT pin

Low voltage protection (VCC pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
ON threshold voltage	Vccon	FA5612: Vcc= 8V to 11V	8.6	9.6	10.6	V
		FA5613: Vcc= 11V to 15V	11.5	13	14.5	V
OFF threshold voltage	Vccoff	Vcc= 11V to 7V	8.0	9.0	10.0	V
Hysteresis	Vcchys	FA5612	0.4	0.6	0.8	V
		FA5613	3.5	4.0	4.5	V

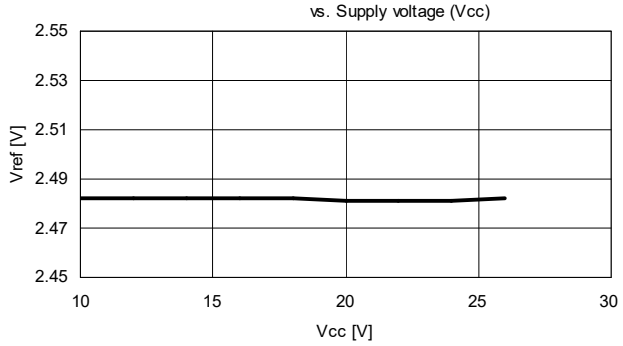
All devices (VCC pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Start-up current	Istart	Vcc = 8V, Vvcmp = 0V Vicmp =0V	70	90	110	µA
Operating current	Icc	OUT pin no load	-	2.0	4.0	mA
OFF time current	Iccoff	OUT pin no load Vvcmp=0V	-	1.8	3.8	mA
Standby current	Istb	Vcc = 18V, Vfb = 0V Vvcmp=0V, Vicmp =0V	80	110	180	µA

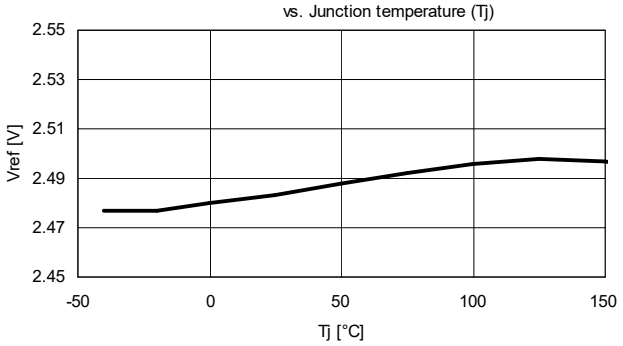
8. Characteristics curves

(Unless otherwise specified, Vfb = 2.5V, Vvcmp = 2.5V, Vvdet = 0V, Vis = 0V, Vicmp = 2.0V, Vcc = 18V, Rg = 4.7kΩ, Tj = 25°C)

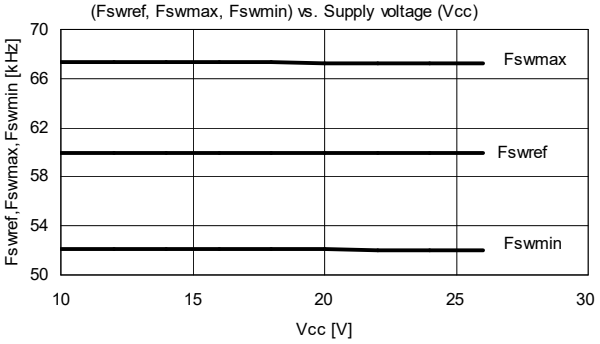
Voltage error amplifier: Input threshold (Vref) vs. Supply voltage (Vcc)



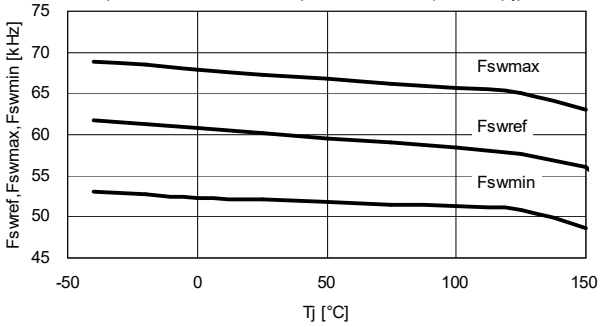
Voltage error amplifier: Input threshold (Vref) vs. Junction temperature (Tj)



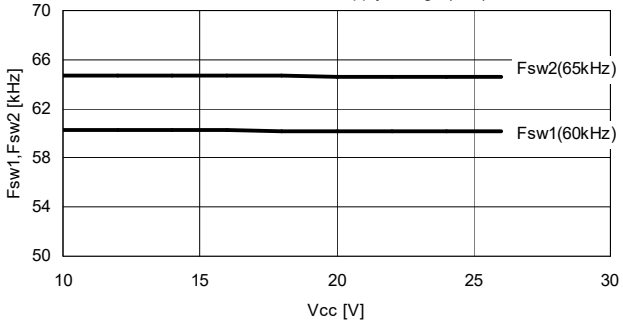
Oscillator: Reference, maximum, minimum frequency (Fswref, Fswmax, Fswmin) vs. Supply voltage (Vcc)



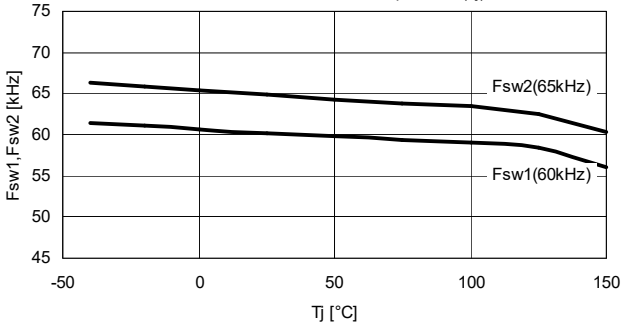
Oscillator: Reference, maximum, minimum frequency (Fswref, Fswmax, Fswmin) vs. Junction temperature (Tj)



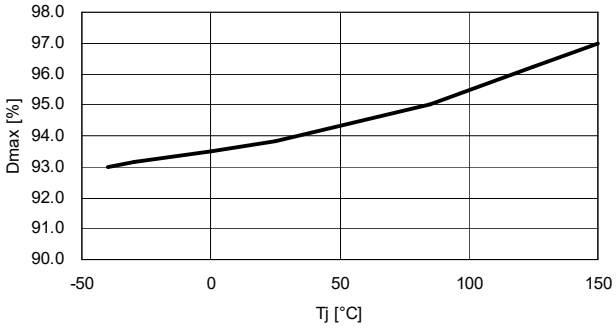
Oscillator: Fixed frequency 1,2 (Fswr1, Fsw2) vs. Supply voltage (Vcc)



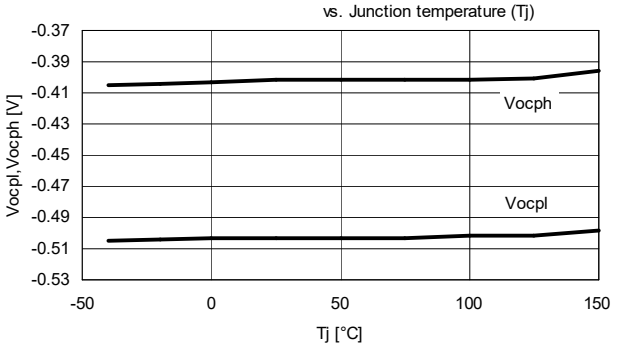
Oscillator: Fixed frequency 1,2 (Fswr1, Fsw2) vs. Junction temperature (Tj)



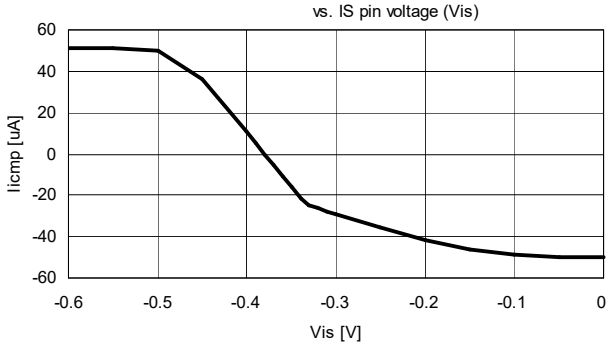
Oscillator: Maximum duty cycle (Dmax) vs. Junction temperature (Tj)



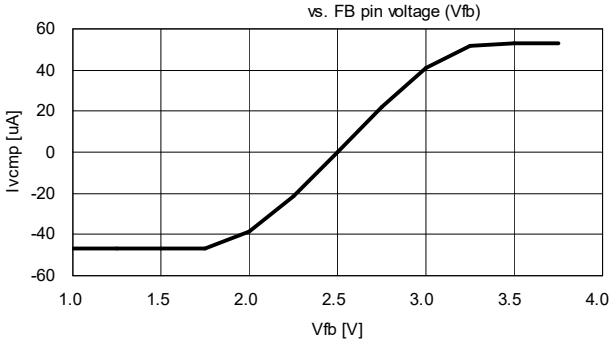
Overcurrent detection: IS threshold voltage (Vocpl, Vovph) vs. Junction temperature (Tj)



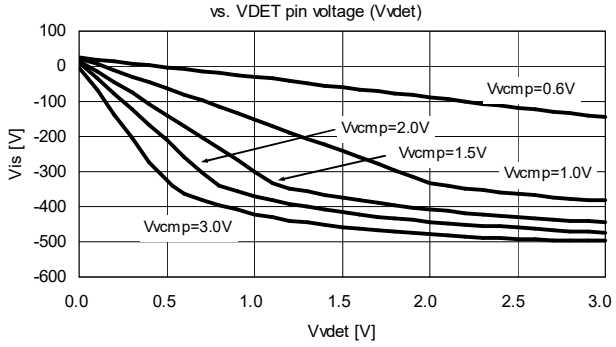
Current error amplifier: Output current (Iicmp) vs. IS pin voltage (Vis)



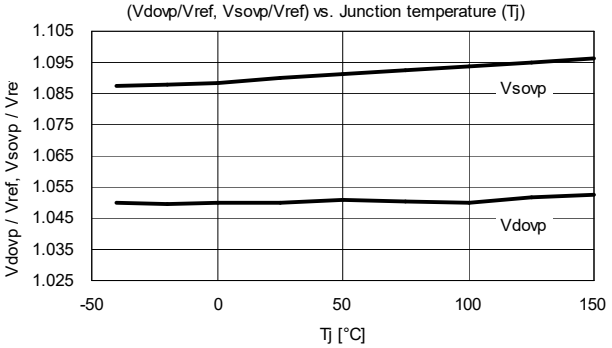
Current error amplifier: Output current (Ivcmp) vs. FB pin voltage (Vfb)



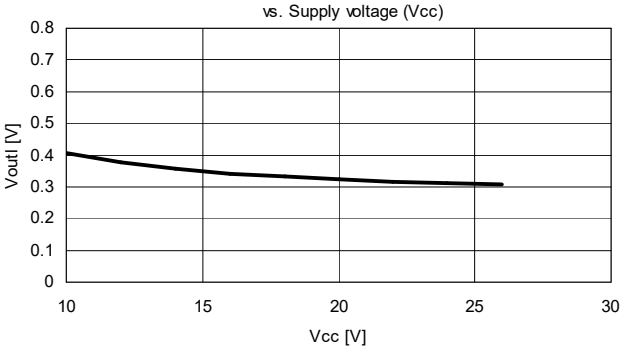
Multiplier: IS pin voltage (Vis) vs. VDET pin voltage (Vvdet)



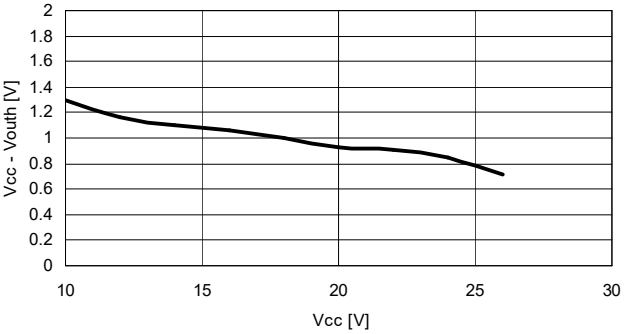
Overvoltage comparator: Dynamic/static OVP (Vdovp/Vref, Vsovp/Vref) vs. Junction temperature (Tj)



OUT pin: Output voltage(L) (VoutI) vs. Supply voltage (Vcc)

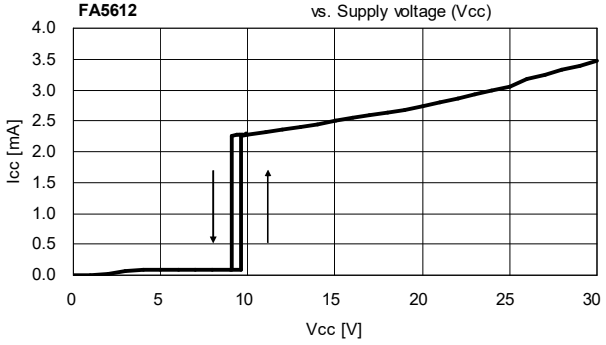


OUT pin: Output voltage(H) (Vouth) vs. Supply voltage (Vcc) Vcc - Vouth



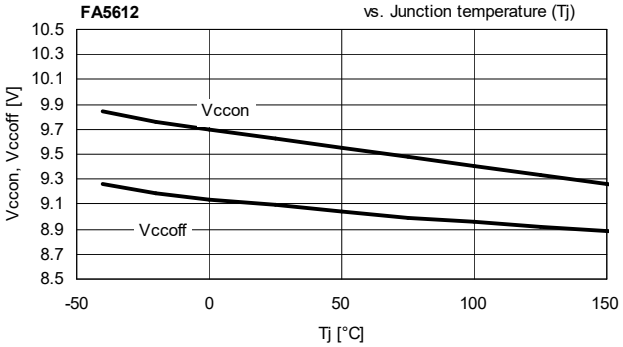
Current consumption: Operating current (Icc) vs. Supply voltage (Vcc)

FA5612



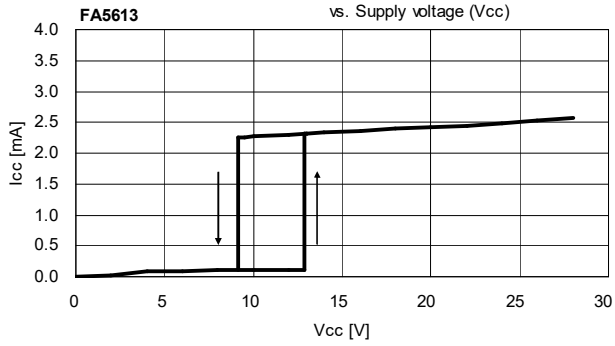
Under voltage lockout: VCC threshold voltage (Vccon, Vccoff) vs. Junction temperature (Tj)

FA5612



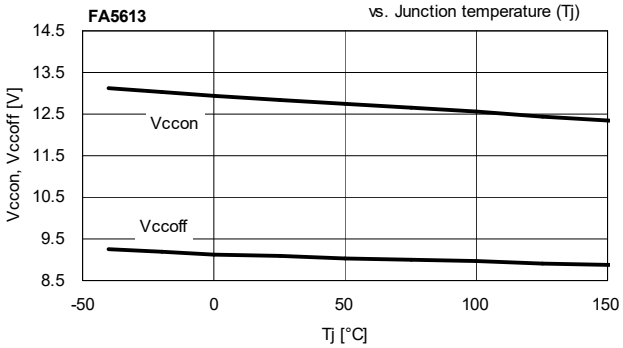
Current consumption: Operating current (Icc) vs. Supply voltage (Vcc)

FA5613

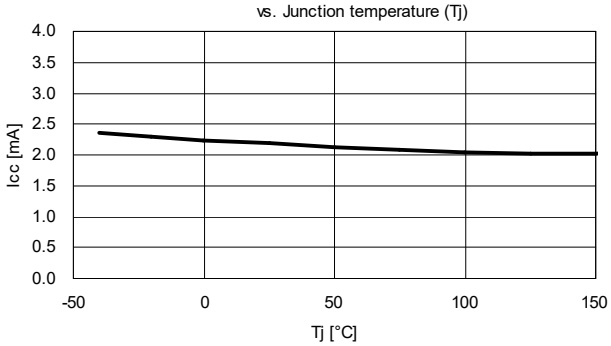


Under voltage lockout: VCC threshold voltage (Vccon, Vccoff) vs. Junction temperature (Tj)

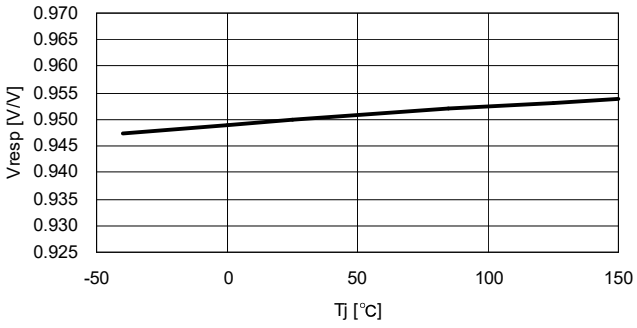
FA5613



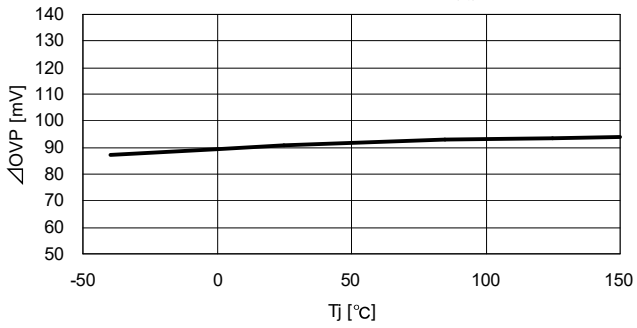
Current consumption: Operating current (Icc) vs. Junction temperature (Tj)



Current error amplifier. Output current (Iicmp) vs. Junction temperature (Tj)



Overvoltage comparator ⊿OVP vs. Junction temperature (Tj)



9. Outline of circuit operation

FA5612/FA5613 are controllers for power factor correction converter using boost topology. These IC are designed for the CCM mode operation with the average current control.
The operations, (1) Switching and (2) Power factor collection, are explained as below with the simplified circuit diagram shown in Fig.1.

(1) Switching operation
Fig. 2 outlines the waveform of each part of switching operation at a steady state. The operation is as follows.
I. Set signal of switching frequency outputted from the oscillator sets RS. F/F, whereby OUT pin voltage goes high, thus turning on Q1. ... (t1)
II. Q1 turned on raises the current of L1. The current of L1 is converted by Rs connected on GND side into a voltage and is inputted to IS pin (VIS). VIS is compared by current amplifier (CUR. AMP) with reference voltage that is obtained via arithmetic output by multiplier (MUL) from input voltage monitoring VDET and VCMP that is obtained by feedback from output and error amplification.
Current amplifier output (ICMP) is compared by PWM comparator (PWM. COMP) with slope waveform outputted from oscillator and, as soon as it attains the reference value, reset signal enters RS. F/F, thereby turning off Q1. ... (t2)
III. Q1 turned off inverts the voltage of L1. While a current is being fed to the output via D1, the current of L1 reduces. Set signal outputted from internal oscillator transfers the circuit to the next switching cycle. ... (t1)

(2) Power factor correcting operation
The voltage at VCMP pin that constitutes output of error amplifier (ERR.AMP) is almost DC voltage at a steady state, because of connected phase compensation capacitance. This voltage is inputted to multiplier. Another input to multiplier is a waveform obtained by rectifying AC input voltage. A multiplier multiplies these two of input and outputs a sinusoidal wave proportional to AC input voltage.
This outputted sinusoidal voltage waveform is applied as a reference inductor current to current amplifier (CUR.AMP).
Therefore, the inductor current's mean value forms a sinusoidal waveform. The current of inductor L1 is deprived of switching ripples by C1 and is turned into a average current. Thus, the current from AC input voltage becomes practically sinusoidal, thus improving the power factor.

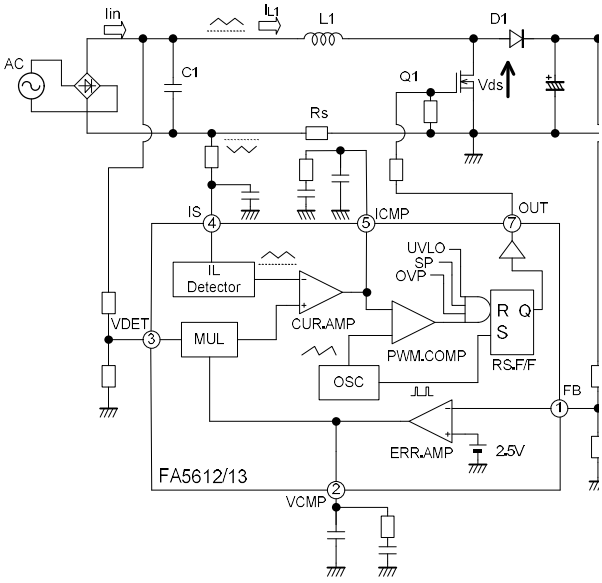


Fig.1 Block diagram of operating circuit

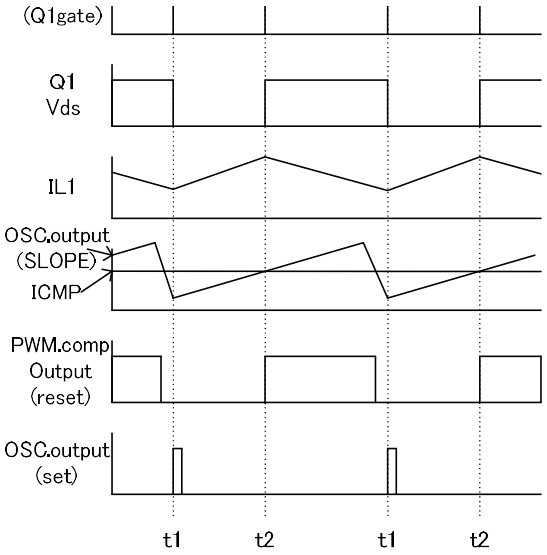


Fig.2 Waveforms of switching operation (outline)

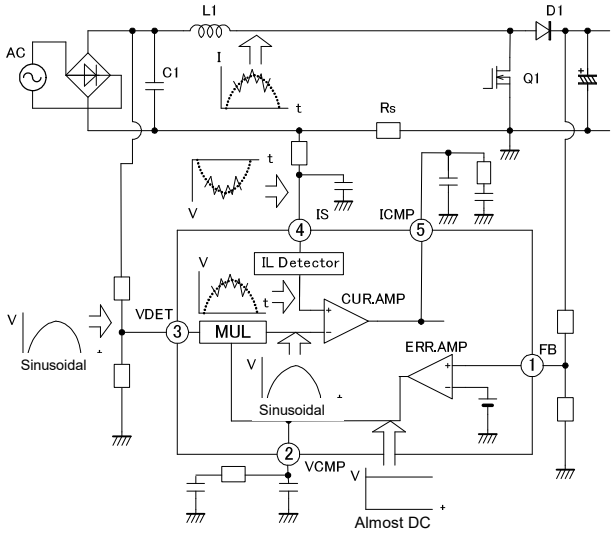


Fig.3 Aspects of waveforms at different parts

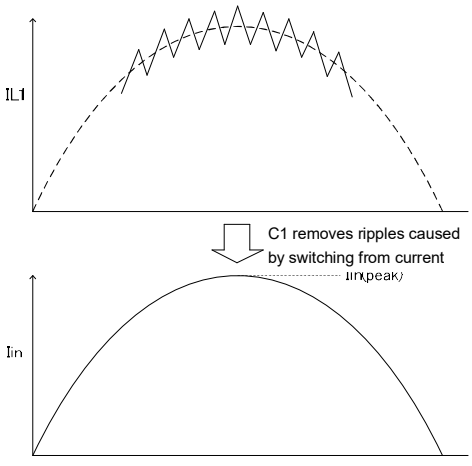


Fig.4 Power factor corrected waveform

10. Description of each circuit block

(1) Frequency setting circuit

The switching frequency is selectable out of 3 modes by resistance Rg connected between OUT and GND pins.

- Mode 1: Frequency diffusion 50 kHz to 70 kHz
- Mode 2: Fixed frequency 1 65 kHz
- Mode 3: Fixed frequency 2 60 kHz

The status setting is completed after FB short detection or UVLO are canceled. The switching operation will start after this completion. Therefore, the mode will not change while operating.

As an example, the operation of frequency setting which is in case of a cancellation of UVLO is shown in Fig. 6.
IC starts to operate after Vcc exceeds Vccon. Then after 5.9ms, the OUT pin outputs current Istate (40mA (typ.)) during 530us.
The current generates a voltage at OUT pin because external resistors (Ro and Rg) are connected to OUT pin.
The frequency setting is done with based on this OUT pin voltage.
The internal circuits start switching operation after frequency setting.

Likewise, in case of cancellation of FB short detection, 5.9ms after the cancellation, a current is outputted from OUT pin for 530us, and then switching starts.

OUT pin has in its inside reference voltages of 2 levels, or Vout1 (310mV (typ.)) and Vout2 (760mV (typ.)) To select a frequency, a reference voltage is compared with OUT pin voltage while current Istate is flowing. The relationship is as follows.

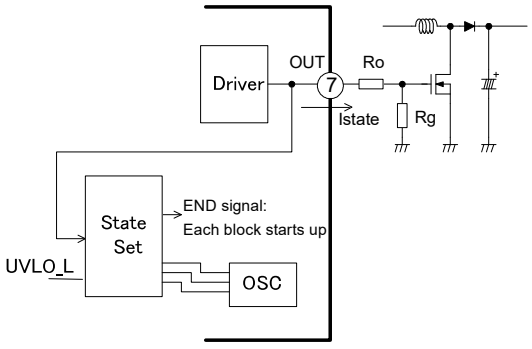


Fig.5 Frequency setting circuit

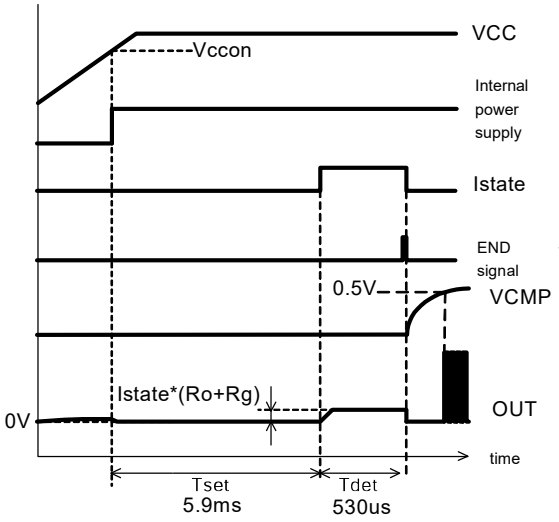


Fig.6 Frequency setting sequence

OUT pin voltage	OUT pin < Vout1	Vout1 < OUT pin < Vout2	Vout2 < OUT pin
Mode	Mode1	Mode2	Mode3
Frequency	Frequency diffusion	Fixed frequency 65kHz	Fixed frequency 60kHz

(2) Oscillator

Oscillator outputs two signals. One is a set signal to flip-flop for setting the OUT pin to Vcc level. Another is a sawtooth signal for PWM comparison.
The oscillation frequency is set by frequency setting circuit to either the frequency diffusion mode or 2 kinds of the fixed frequency mode.

(2-1) Frequency diffusion
When the frequency diffusion mode is selected, the frequency changes between 50 and 70 kHz according to the input/output status of PFC power supply. The optimized frequency diffusion based on input/output status realizes a low noise operation with a wide operation range.
OSC block determines the frequency based on VDET pin input voltage and multiplier block output voltage. When the phase angle is range of 0° to 30° or 150° to 180° approximately, the frequency rises in proportion to VDET pin voltage. When it is range of 30° to 150° approximately, the frequency is reversely proportional to the multiplier output. (Fig.8)
When the multiplier output is high like when PFC output current is large, the frequency drop is bigger. And it is small in case of reverse situation.

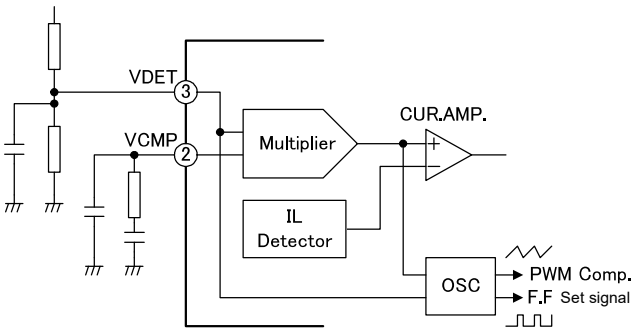


Fig.7 Block diagram for oscillator area

The approximate frequency (Fsw_b) is given by an equation below when the phase angle is range of 30° to 150°.

Fsw_b = 75 – 71.4 × (IS pin voltage) [kHz]

(2-2) Maximum and minimum frequencies in frequency diffusion mode

As stated above, the switching frequency in the frequency diffusion mode depends on VDET pin or multiplier output voltage within maximum and minimum frequencies determined. However, maximum or minimum frequency may never appear under some conditions while 1/2 of AC cycle.

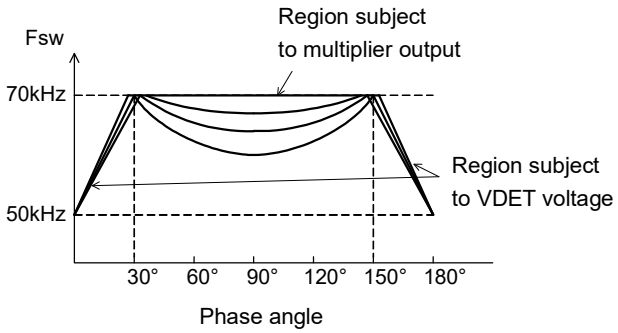


Fig.8 Oscillation frequency vs. phase angle

(3) Error amplifier

The error amplifier is a circuit for controlling PFC output to a certain level. This IC adopts a transconductance amplifier.

The non-inverting input terminal for the error amplifier is connected to the internal reference voltage of 2.5 V (typ.) The inverting input terminal (FB) receives the output voltage, usually resistively divided, from power factor correction converter. For FB open detecting function, this terminal is connected to a pull-down resistor of 2.5MΩ inside the IC. Error amplifier output (VCMP) is connected to multiplier (MUL) to control the inductor current.

Output voltage Vout of power factor correction converter usually contains a lot of ripples of double the AC line frequency (50 or 60 Hz). When ripples corresponding to double the AC frequency appear excessively on the error amplifier output, power factor correction converter will not operate stably. So, a capacitor and resistor network is connected between pin 2 (VCMP) which is output of the error amplifier and GND for phase compensation.

Increasing the capacitance in the phase compensation network improves the power factor, but the transient responsivity becomes slow.

The error amplifier in FA5612/13 has a function of improving the transient responsivity.

When the load has suddenly become so heavy, the FB pin voltage drops much. If lowered FB pin voltage is below transient response detection voltage (Vresp), the transient response correction circuit increases output current of error amplifier up to the transient response output current (Iresp). Thus, the VCMP pin voltage rises quickly to increase the output current and suppress the output voltage drop.

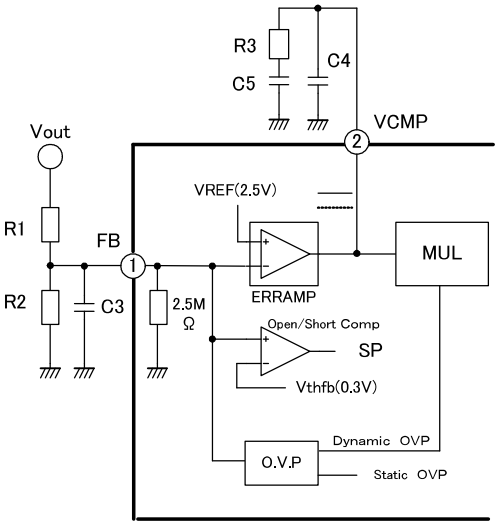


Fig.9 Error amplifier and overvoltage protection circuit

(4) Overvoltage protection circuit (OVP)

This is a circuit for limiting the voltage when the output voltage of power factor correction converter has exceeded the setting.

When converter is started up or when the load has suddenly changed, the converter output voltage may rise beyond the setting. In such a case, OVP circuit prevents an over voltage and protects the converter.

FA5612/13 has a dynamic OVP function and a static OVP function. The dynamic OVP function restricts the multiplier gain depending on rising of FB pin voltage while FB pin voltage exceeds 2.5 V. The static OVP function makes OUT pulses stop while FB pin voltage exceeds 1.09 time of the reference voltage.

In normal operation, the FB pin voltage is 2.5 V that is almost the same as the reference voltage of error amplifier.

When the FB pin voltage exceeds 2.5 V by startup or a sudden change of load, the dynamic OVP function reduces output current by lowering the multiplier gain. Then, if the FB pin voltage still rises and exceeds the reference voltage of a static OVP function, FA5612/13 stops the output pulses.

OUT pulses stopped by the overvoltage protection are resumed as soon as the output voltage lowers back to 1.07 times the reference voltage.

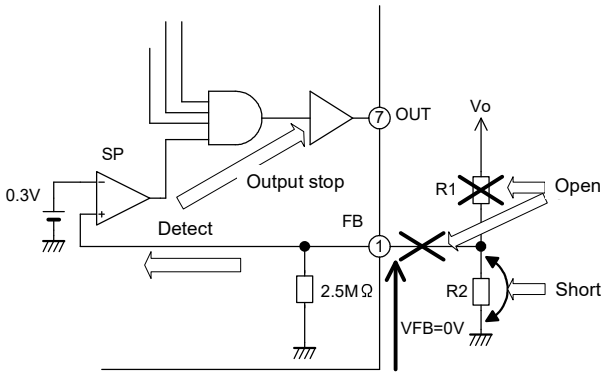


Fig.10 FB open/short detector

(5) FB short/open detector

On the circuit of Fig. 10, if the FB pin voltage is zero because of R2 short or R1 open, the error amplifier can not control the constant voltage. Therefore, the output voltage rises abnormally. In such a case, the overvoltage protection circuit could not operate because the output voltage detection is faulty.

To avoid such inconvenience, the IC has FB short detector.
The circuit consists of reference voltage of 0.3 V (typ.) and comparator (SP).
When the FB pin input voltage has dropped below 0.3 V because of R2 short or R1 open, the output of comparator (SP) is inverted to stop the IC output.

The PFC converter outputs a voltage corresponding to the input voltage even before startup because of the boost topology. That is why, this function never operate as long as the converter is normal.
In case of an open failure of the FB pin FA5612/13 stops the output pulse by this function because a pull-down resistor of 2.5 MΩ inside the IC is connected to the FB pin.
If the FB pin voltage has dropped to almost zero, the IC output will stop. When the FB pin voltage returns normal then, OUT pulses will reappear.

(6) Multiplier

Multiplier is the circuit for controlling the input current as the sinusoidal wave forms the same as input voltage.
An input is connected to VDET pin and is inputted the dividing voltage after being rectified from AC input voltage. The other input is connected to error amplifier output (VCMP). Normally, the error amplifier output is almost DC, and multiplier outputs a sinusoidal waveform voltage whose amplitude changes according to the error amplifier output voltage. The multiplier output constitutes a reference for current comparator to control the input current to a sinusoidal waveform (Fig. 11).

It usually makes MUL pin peal voltage set to 0.65 to 2.4 V in the all AC input range.
The voltage obtained by rectifying the AC input voltage contains many noises attributable to switching by Q1. To eliminate the influence by the noise, filtering capacitance C6 is provided usually.

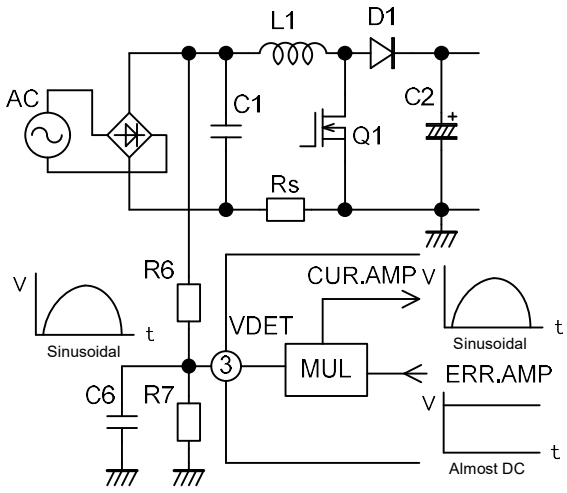


Fig.11 Multiplier

(7) Current detector

IL. Detector inverts and amplifies a voltage obtained by voltage-current conversion via current detecting resistance Rs of the inductor current.
Current amplifier (CUR. AMP) is error amplifier that composes a current loop to make the input current follow a sinusoidal waveform.
Current amplifier receives IL. Detector output and multiplier (MUL) output, subjects them to comparison and error amplification, and outputs the result to PMW comparator (PWM. COMP).
Current amplifier is a transconductance amplifier the same as error amplifier. Capacitance and resistance connected between output terminal (ICMP) and GND for phase compensation eliminate switching ripples of the input current.
The current detector output is clamped to Vclamp: 2.7 V by clamp circuit that constitutes an upper limit of voltage.

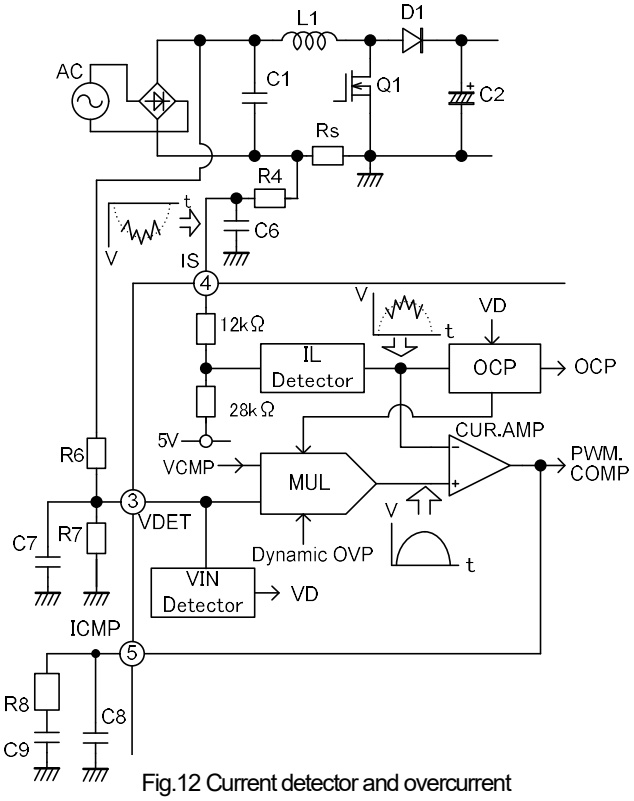


Fig.12 Current detector and overcurrent protection circuit

(8) Overcurrent protection circuit (OCP)

OCP circuit is the circuit to detect the inductor current, and is to stop the output pulse to protect MOSFET when detected current exceeds certain intensity.
A detected voltage by sense resistor Rs connected to GND is inputted to the IS pin, is converted by the IL_Detector which is an inverting amplifier, and is compared by overcurrent detection comparator. When IS pin voltage lowers below a threshold value (OCP level), overcurrent protection circuit outputs a signal of an overcurrent status.
The signal of overcurrent status resets a flip-flop for the OUT pulse, and then turns MOSFET off.
When IS voltage gets near a threshold value, overcurrent protection circuit lowers the gain of multiplier (MUL) to suppress the input current, thereby suppressing the audible noise of inductor attributable to an overcurrent.

OCP level is changed depending on the peak voltage of VDET pin by VIN_Detector as follows.
While period A, OCP level is set to Vocph (-0.4 V) because VDET pin voltage exceeds threshold voltage Vvdeth (1.6 V). OCP level is changed only when VDET pin voltage is below Vvdets (0.3V). At this time, the inductor current is low enough, and therefore will not abruptly change. Further, if the load current is very low such VDET will not be below 0.3 V, the OCP level will not change over regardless of VDET.

During period B, VDET will never go below threshold voltage Vvdetl: 1.35 V. Therefore, OCP level will not change either.
Some time in period C, VDET will be below threshold voltage Vvdetl: 1.35 V, whereby OCP level is set to Vocpl (-0.5 V). The same as period A, OCP level is changed only when VDET pin voltage is below Vvdets (0.3 V).

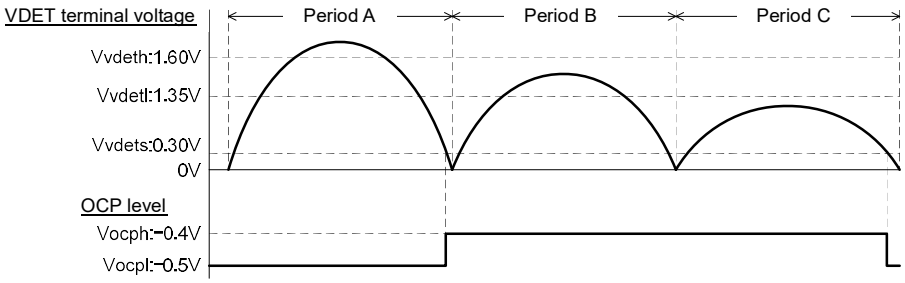


Fig.13 Overcurrent protection (OCP) level and VDET voltage

(9) Undervoltage lockout circuit (UVLO)

FA5612/13 has the UVLO circuit to avoid unexpected operation when the source voltage has dropped.
The IC starts operation when the source voltage rising from zero has reached 9.6 V (typ.) for FA5612, or 13 V (typ.) for FA5613.
After startup, each of ICs stops operating when the source voltage has dropped to 9 V (typ.)
While the IC stops a switching operation by UVLO circuit, the IC keeps OUT pin voltage low and further reduces IC consumption current to below 100 μA.

(10) Output circuit

The output circuit consists of a push-pull circuit, directly drives MOSFET.
Its maximum peak current is 1.5 A for sink, and 1.5 A for source.

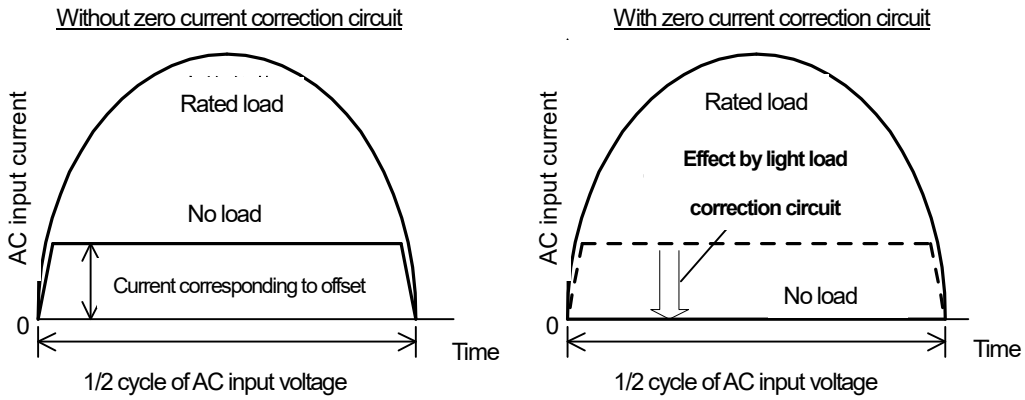
(11) Zero current correction circuit

Unless multiplier output or current error amplifier input has offset voltage, the input current to converter will be almost zero when PFC converter has completely no load.
However, if the offset voltage viewed from IS pin is negative, the input current corresponding to offset voltage might flow to converter even when no load or light load. In such a case, the output voltage of power factor correction converter will rise abnormally because the input current will be excessive.
Offset voltage in the IS pin (Visof) is 0 mV. However, the offset voltage of the IS pin against sense resistor voltage may be negative because a voltage will be generated by an external filter resistance connected to the IS pin. Therefore, FA5612/13 has this correction circuit to avoid rising the output voltage when light load with such case.

Usual output voltage from error amplifier is 0.5 V or higher. When its output voltage has dropped below 0.5 V, zero current correction circuit operates.
Error amplifier output voltage drops below 0.5 V when an input current flows under no or light load on account of offset in multiplier output or current error amplifier input. Then, zero current correction circuit corrects the offset voltage of multiplier output. This function prevents the output voltage of power factor correction converter from rising excessively, so that the output voltage is kept at a constant level.
The correction amount varies in a linear function of the output of current error amplifier, thereby ensuring a stable run.
Fig. 14 shows effects of zero current correction circuit.

Consumption diagram of operations when IS pin offset is negative

Input current



Output voltage

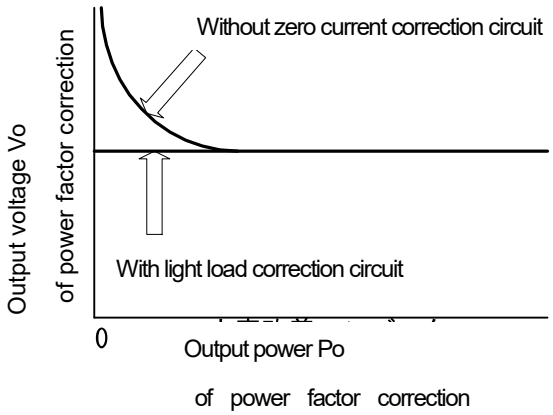


Fig.14 Effects of zero current correction circuit

11. Description of use for each pin

(1) Terminal No.1 (FB pin)

Functions

(i) Inputs feedback signal of output voltage setting

(ii) Detects FB pin open/short

(iii) Detects output overvoltage state

Applications

(i) Feedback signal input

▪ Wiring

Connect the node of dividing resistance for output voltage setting

▪ Operation

The PFC output voltage is controlled so that the FB pin voltage will correspond to the internal reference voltage (2.5 V).

For FB pin open circuit, FB pin is connected with pull-down resistance in IC inside. Therefore, take its resistance into account when choosing the resistance of R1 and R2 to set the output voltage (Vout).

$$Vout = (R2 + Rfb)/(R2 \times Rfb) \times VREF \times R1 + VREF$$

where:

VREF: Reference voltage = 2.5 V (typ.)

Rfb: FB pin pull-down resistance = 2.5 MΩ (typ.)

To avoid an erratic operation by noises, connect capacitance C3 of 100 to 3300 pF between FB pin and GND.

(ii) FB pin open/short detection

▪ Wiring

Same as feedback signal input in (i)

▪ Operation

When, on account of FB pin open circuit or short circuit of R2 in resistive divider, the FB input voltage has dropped below 0.3 V, the output of comparator (SP) is inverted, thereby stopping the IC output.

(iii) Output overvoltage detection

▪ Wiring

Same as feedback signal input in (i)

▪ Operation

In normal operation, FB pin voltage is almost the same as reference voltage of error amplifier (2.5 V). Like when the output voltage has risen for some reason, if the FB pin voltage reaches comparator reference voltage (1.09*VREF), comparator (OVP) output is inverted to stop OUT pulses. As soon as output voltage returns to a normal level, OUT pulses are recovered.

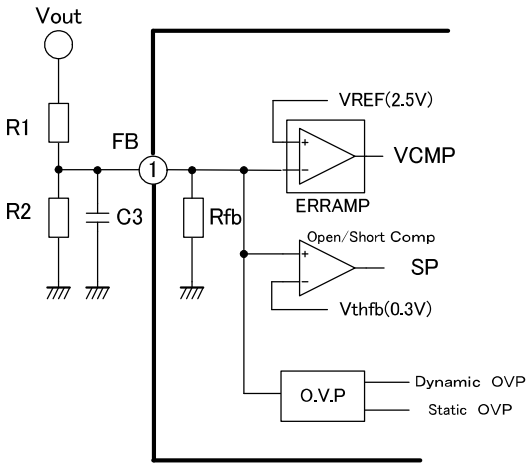


Fig.15 FB pin circuit

(2) Terminal No.2 (VCMP pin)

Function

(i) Phase compensation of output of incorporated voltage error amplifier (ERRAMP)

Application

(i) Phase compensation of incorporated ERRAMP output

▪ Wiring

Connect R and C between COMP and GND as shown in Fig. 16

▪ Operation

COMP pin avoids an appearance of the double frequency ripple of the AC line on the FB pin voltage with connecting R and C.

Reference:

Example of applied circuit: C4 = 0.47 uF
C5 = 2.2 uF
R3 = 10 kΩ

The above is an example. Determine them upon sufficiently verifying your instrument.

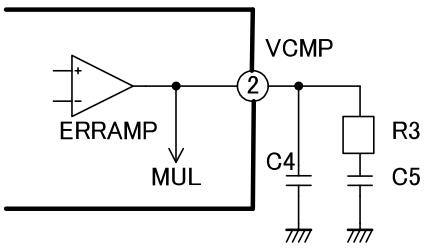


Fig.16 VCMP pin circuit

Besides, Soft start function is realized by slowing a voltage rise of COMP pin with adjustment of capacitance connected between COMP and GND.
When starting, VCMP voltage rises and a switching operation starts at 0.5 V.
At this time, MOSFET ON width increases gradually in proportion to the COMP voltage rise. The soft start time is adjustable with adjustment with changing capacitors C4 and C5.

Increasing C4, C5 capacitance → prolongs soft start time
Decreasing C4, C5 capacitance → shortens soft start time

(3) Terminal No.3 (VDET pin)

Function
(i) Input voltage detection (multiplier input)
Application
(i) Input voltage setting for VDET pin
Multiplier generates current reference signal. Its VDET pin (pin 3) receives sinusoidal full-waveform rectified waveforms. Considering the dynamic range of multiplier operation, VDET pin peak value would be used within 0.65 to 2.4 V. Therefore, set R6 and R7 in Fig. 17 so that the peak voltage of sinusoidal waveforms at VDET pin will be between 0.65 and 2.4 V with the entire range of AC input voltage.

Recommended dividing ratio: R6:R7 = 160:1

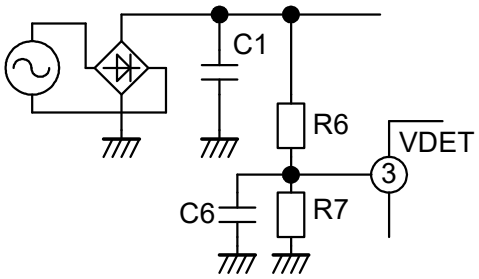


Fig.17 VDET terminal circuit

Caution:
Because multiplier has dispersions of characteristics, even if VDET pin voltage is 2.4 V or lower, multiplier might be saturated and the input peak current would slightly be truncated like trapezoidal waves.

(4) Terminal No.4 (IS pin)

Functions
(i) Inductor current detection
(ii) Turn off OUT output upon detecting an overcurrent
Applications
(i) Via IS pin, inductor current signal is applied to current error amplifier (CUR_AMP) that constitutes a current loop for making the input current follow sinusoidal waveforms. CUR_AMP that is connected with multiplier output receives current reference signal. IS pin is current input terminal, and receives a potential of 0 to -0.4 V with respect to GND level.
(ii) When IS pin voltage is lower than IS threshold voltage, comparator output signal is inverted to turn off OUT output.
▪ Supplement
When MOSFET turns on, MOSFET gate drive current and surge current are generated by discharge of stray capacitance, and then those currents flow to current detecting resistance Rs. An excessively large surge current may cause an erratic operation to disturb the input current waveform. Depending on the surge current intensity, timing, etc., pulse shoots may mix with turn-on parts of IC's OUT pulses. So, RC filter shown in Fig. 18 is connected in generally.
Since the level is determined by resistive division as shown in Fig. 18, 100 Ω or lower is recommended for input resistance R4.
Rated voltage at IS pin for input of inductor current signal is -5 V.
In case of a general boost circuit, a rush current flows for charging the output smoothing capacitance C2 the instant an AC input voltage has been connected. This current may be considerably greater than at a steady operation.
As a result, IS pin may receive a voltage that is far higher than usual. Even if such AC voltage is connected, IS pin must not be exposed to a potential higher than -5 V that is an absolute maximum rated voltage.
There may be the case that a voltage higher than the rated is applied to IS pin. In such case, it needs to use a preventive circuit for suppression of a rush current or to add the Zener diode to IS pin as shown in Fig. 19.

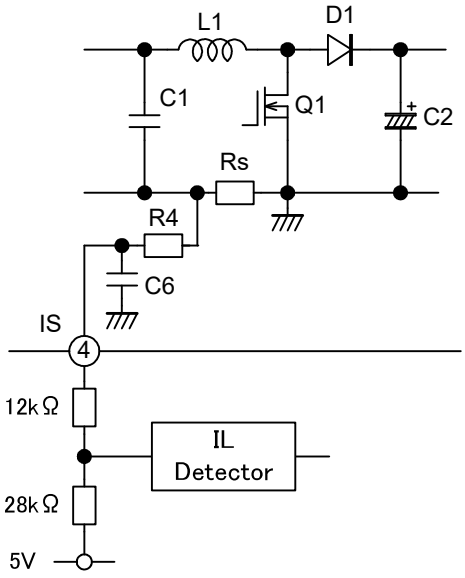


Fig.18 IS pin circuit

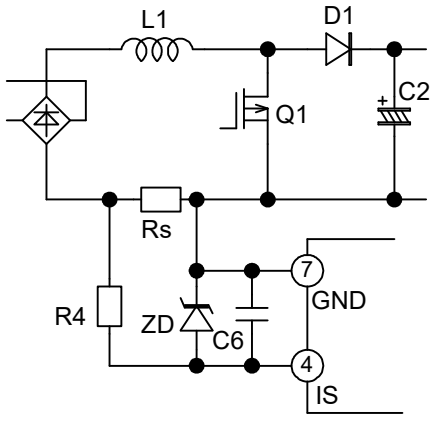


Fig.19 IS pin circuit (2)

Caution:

Maximum power design

It needs a notice about a setting of the sense resistance to output maximum power at whole input condition because a power limitation may occur by IC functions.

Fig. 20 shows a block diagram concerning the input current control.

The VDET voltage is relatively high at high RMS input voltage, and the input current is limited by OCP function shown in the path B of Fig. 20 in such case. (Reference figure is shown in Fig. 21.)

The VDET voltage is relatively low at the low RMS input voltage, and the maximum output voltage of multiplier is low too. So, the input current is limited by the multiplier shown in the path A of Fig. 20 in such case. (Reference figure is shown in Fig. 22.)

This means that the maximum inductor current is limited by an above function unless the reasonable sense resistance is chosen.

Therefore, it needs to choose the sense resistor Rs which satisfies each condition shown in the next page.

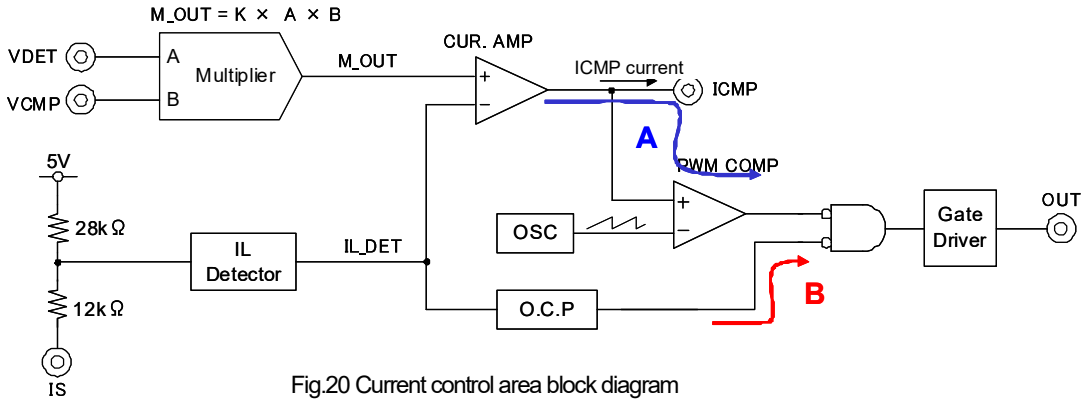


Fig.20 Current control area block diagram

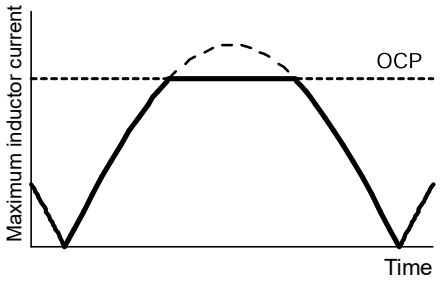


Fig.21 Maximum inductor current at high input voltage

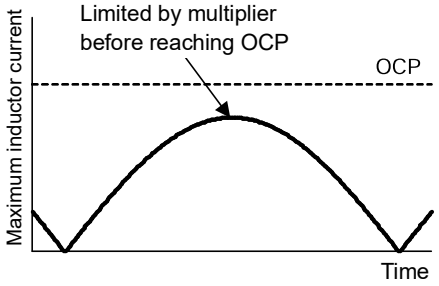


Fig.22Maximum inductor current at low input voltage

Note that the limitation of maximum inductor current is different as shown in Fig. 23 according to whether by OCP or by multiplier.

- By OCP: Current peaks including switching ripples are subjected to limitation.
- By multiplier: Current excluding switching ripples is subjected to limitation.

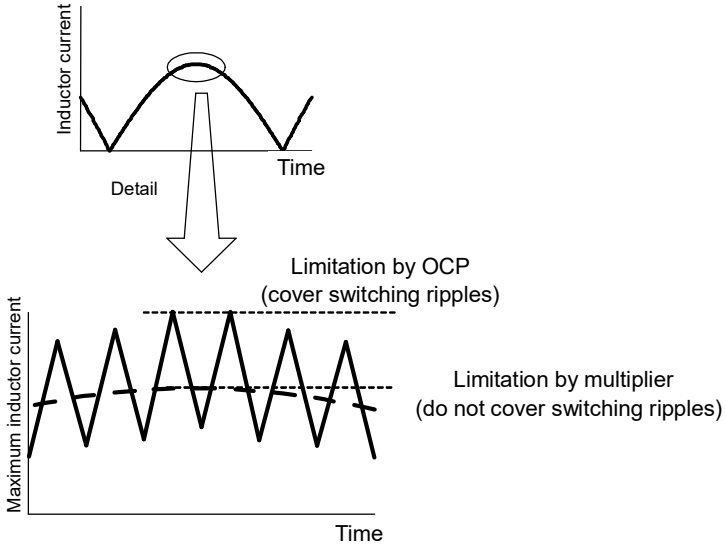


Fig.23 Maximum current limitation

Design current detecting resistance Rs so as to meet a maximum power in the input voltage range, and also to clear 2 power limiting conditions below (Fig. 24).

(1) Power limitation by multiplier

Design current detecting resistance Rs so that VIS voltage (mean) will be -0.33 V or greater that is maximum of item " IS pin voltage (Vis_054) ".

In case of settling as output power Po (W), efficiency η, and minimum input voltage Vacmin (V), maximum inductor current Iinmax (A) is given by following equation.

$$Iinmax = \sqrt{2} \cdot \frac{Po}{\eta \times Vacmin}$$

VIS voltage (mean) will be -0.33 V or higher when:

$$-Rs \times Iinmax \ > -0.33V$$

$$-Rs \times \sqrt{2} \cdot \frac{Po}{\eta \times Vacmin} \ > -0.33V$$

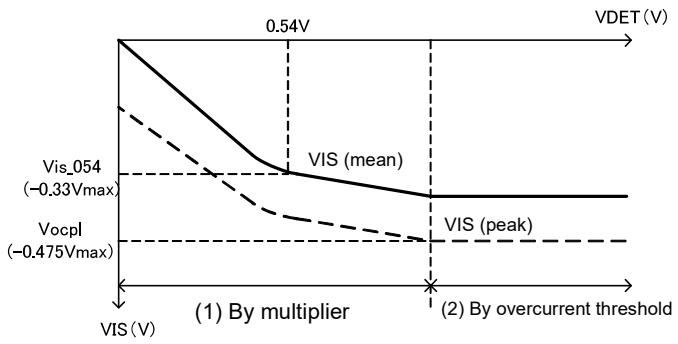


Fig.24 Maximum power limitation

Therefore, design current detecting resistance Rs (Ω) so as to meat:

$$Rs < \frac{0.33 \times \eta \times Vacmin}{\sqrt{2} \times Po} (\Omega) \quad \text{..... (1)}$$

(2) Power limitation by OCP

Design current detecting resistance Rs so that VIS voltage (peak) will be -0.475 V or greater that is maximum of IS threshold voltage (Vocpl).

In case of settling as ripple current Iripple (A), switching frequency fsw, output voltage Vout, boost inductance L, and ON duty D, ON duty D is given by following equation.

$$D = \frac{Vout - \sqrt{2}Vac\,min}{Vout}$$

VIS voltage (peak) will be -0.475 V or higher when:

$$-Rs \times (Iinmax + \frac{Iripple}{2}) \ > -0.475V$$

$$-Rs \times (\frac{\sqrt{2} \times Po}{\eta \times Vacmin} + \frac{\sqrt{2} \times Vac\,min \times D}{2 \times fsw \times L}) > -0.475V$$

Therefore, design current detecting resistance Rs (Ω) so as to meat:

$$Rs < \frac{0.475}{\frac{\sqrt{2} \times Po}{\eta \times Vacmin} + \frac{Vac\,min \times D}{\sqrt{2} \times fsw \times L}} \ (\Omega) \text{ ..... (2)}$$

In order to output maximum power at a minimum input voltage, therefore, select Rs determined by expression (1) or (2), whichever smaller.

Caution:

To define a current limitation by multiplier, select the voltage at VDET pin so as to be 0.54 V or higher even at a minimum input voltage.

(5) Terminal No. 5 (ICMP pin)

Function

(i) Phase compensation for output of incorporated current error amplifier (CUR_AMP)

Application

(i) Phase compensation for output of incorporated CUR_AMP

▪ Wiring

Connect R and C between ICMP and GND as shown in Fig. 25.

▪ Operation

R and C are connected to ICMP pin to block ripple components of switching frequency that could otherwise appear on IS pin input.

(Reference)

Example of applied circuit: C8 = 100 pF

C9 = 680 pF

R8 = 47 kΩ

The above is an example. Determine them upon sufficiently verifying your instrument.

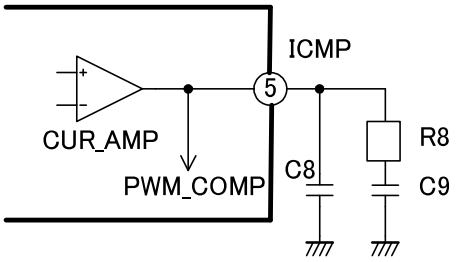


Fig.25 ICMP pin circuit

(6) Terminal No. 6 (GND pin)

Function

Constitutes the reference of each part of IC.

(7) Terminal No. 7 (OUT pin)

Functions

(i) Drives MOSFET

(ii) Sets oscillation frequency

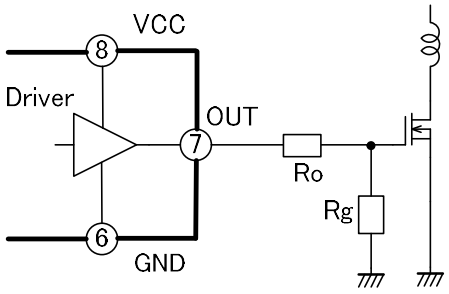


Fig.26 OUT pin circuit (1)

Applications

(i) Drive of MOSFET

▪ Wiring

Connected via resistance Ro to gate terminal of MOSFET

▪ Operation

Goes high when MOSFET is turned on. Nearly VCC voltage is outputted.

Goes low when MOSFET is turned off. Voltage of nearly 0 V is outputted.

▪ Supplement

Connect a gate resistance for current limitation at OUT pin, prevention of oscillation of gate terminal voltage, etc.

Rated output currents of IC: Source ... 1.5 A, sink ... 1.5 A.

Connection in Fig. 27 or 28 allows to distinctly set the gate drive currents for turning on and off MOSFET.

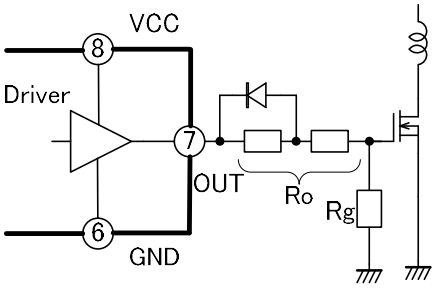


Fig.27 OUT pin circuit (2)

(ii) Setting of oscillation frequency

▪ Wiring

(1) Ordinary connection

Connect resistance Rg between MOSFET gate and GND if no buffer is connected on IC output as shown in Fig. 26, 27 and 28. According to resistance Rg, switching frequency can be selected out of 3 different modes given in table below.

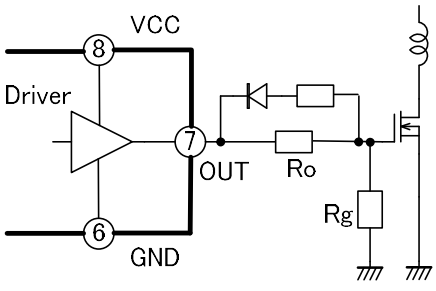


Fig.28 OUT pin circuit (3)

		Resistance Rg	Accuracy	Temperature characteristics
Mode1	Frequency diffusion	4.7kΩ	±5%max	200ppm/°Cmax
Mode2	65kHz fixed	12kΩ	±2%max	200ppm/°Cmax
		13kΩ	±5%max	200ppm/°Cmax
Mode3	60kHz fixed	27kΩ	±5%max	200ppm/°Cmax

* Ro: 100 Ω max.

Caution:

▪ Resistance Ro between OUT pin and FET gate must be 100 Ω or less

▪ If mode 3 is selected (27 kΩ used), starting up the frequency setting raises the OUT-GND voltage up to 1.4V

(2) If buffer is connected on IC output

If buffer is connected on IC output, select a configuration shown in Fig. 29, and select the frequency setting resistance as given in table below.

		Resistance Rg	Accuracy	Temperature characteristics
Mode1	Jittering	4.7kΩ	±5%max	200ppm/°Cmax
Mode2	65kHz fixed	13kΩ	±5%max	200ppm/°Cmax
Mode3	60kHz fixed	30kΩ	±5%max	200ppm/°Cmax

* Ro: 100 Ω max.

If combined resistance connected on buffer output is Rx, set Rx to 3 kΩ or higher taking into account dispersion and temperature characteristics.

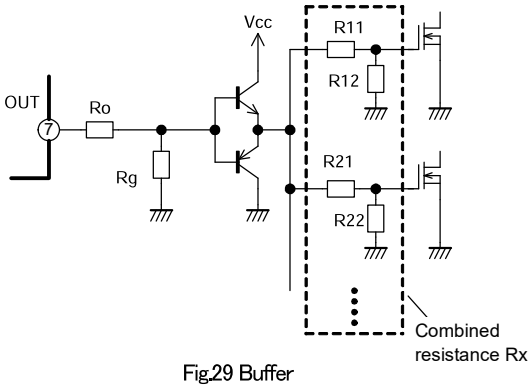


Fig.29 Buffer

Example:

Select R11 = 10 Ω, and R12 = 10 kΩ. Suppose their resistance may change by 10% maximum on account of their dispersion and temperature characteristics. If 3 of them each are connected in parallel,

Rx = 10.01 kΩ × 90% ÷ 3 = 3.003 kΩ

holds, thereby clearing the requisite.

Caution:

- Resistance Ro between OUT pin and buffer must be 100 Ω or less
- If mode 3 is selected (30 kΩ used), starting up the frequency setting raises the OUT-GND voltage up to 1.2 V
- Above conditions presuppose h_{FE} of transistor used in buffer is 50 minimum, and that Vbe is 0.3 V maximum taking the temperature characteristics into account. Unless characteristics of a particular transistor to use clear the requisites, set the frequency resorting to a method in "(3) Other circuit configuration."

(3) Other circuit configuration

Unless the circuit configuration connected to OUT pin clears the specifications in (1) nor (2), determine the frequency based on the current and voltage defined by specified frequency setting.

(See p. 15 Fig. 5 Frequency setting circuit)

Be sure to take into account the IC characteristics, and dispersion and temperature characteristics of parts connected to OUT pin.

General precaution about frequency setting:

In setting the frequency, make sure, in addition to respecting our recommendations in (1) and (2) above, there is no problem of influences by dispersion and temperature characteristics of your resistors, wiring, noise (influence of auxiliary power supply that operates before PFC starts, in particular) and other matters than resistance itself based on the current and voltage regarding the specified frequency setting.

In setting of the frequency, please confirm whether there is no bad influence of following items including our setting recommendation and our setting specification.

- Dispersion of or the temperature characteristic of resistance used, a design of wiring, noise (especially from sub power supply before the PFC start operation), etc.

(8) Terminal No. 8 (VCC pin)

Function

(i) Supplies IC with power

Application

(i) Supplies IC with power

▪ Wiring

Connect a startup resistance between rectified voltage line and VCC pin.

Generally, connect a rectified and smoothed voltage from auxiliary winding provided on transformer.

Or connect an external DC source.

▪ Operation

At the time of startup in case VCC voltage is obtained from auxiliary winding, the current via the startup resistance charges the smoothing capacitance and, when the level rises up to UVLO ON threshold voltage, IC starts up. Immediately before startup, a current of at least 110 uA (max.) that is a startup current for IC must be fed. During a steady operation, VCC is supplied from inductor's auxiliary winding (Fig. 30).

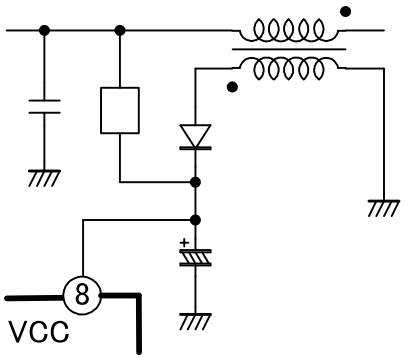


Fig.30 VCC pin circuit (1)

As the source voltage rises from zero, the operation starts at 9.6 V (typ.) for FA5612, or at 13 V (typ.) for FA5613.

Any of started-up ICs stops operating when the source voltage drops down to 9 V (typ.)

While IC stops operation by under voltage lockout circuit, OUT pin keeps low level and shuts the output of power supply off.

Supplement:

Under voltage lockout function avoids an erratic operation of circuit when source voltage has dropped.

Noise applied to VCC pin will cause an erratic operation. To avoid the noise, connect a capacitance near VCC pin whether IC is operated by another source or not. Determine the capacitance so that the noise generated on VCC pin will be within ±0.6 V, and make doubly sure no erratic operation occurs by noise (Fig. 31).

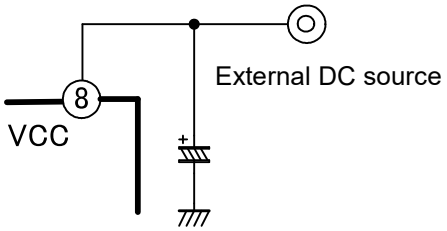


Fig.31 VCC pin circuit (2)

12. Advice for design

(1) Advice in pattern designing

Main circuit MOSFET, inductor, diodes, etc. perform switching under high voltage and large current. If wiring of IC or signals inputted to IC gets too near such main circuit parts, they may operate erratically upon being affected by noise generated there.

Attention must be paid particularly in following cases (examples of faulty cases).

- IC is arranged under inductor or other main circuit parts, or immediately behind main circuit parts on double sided circuit board (Fig. 32)
- IC is arranged close to inductor, MOSFET or diode (Fig. 33)
- Signal wiring is placed under inductor or near MOSFET or diode (Fig. 34)

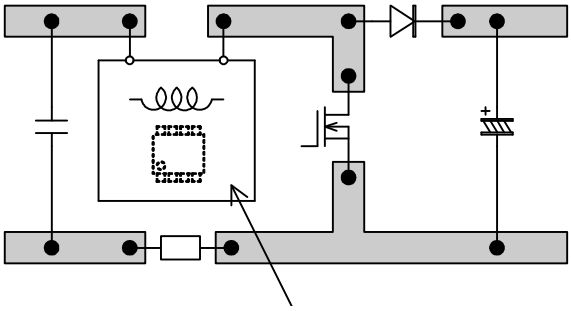


Fig.32 Example of inadvisable arrangement (1)

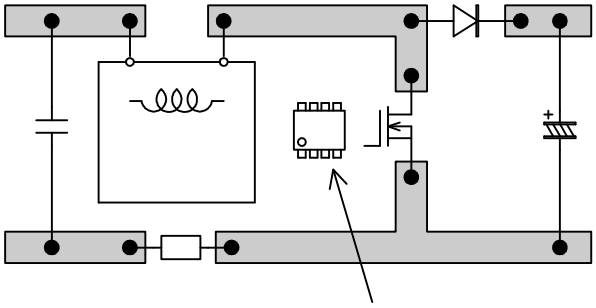


Fig.33 Example of inadvisable arrangement (2)

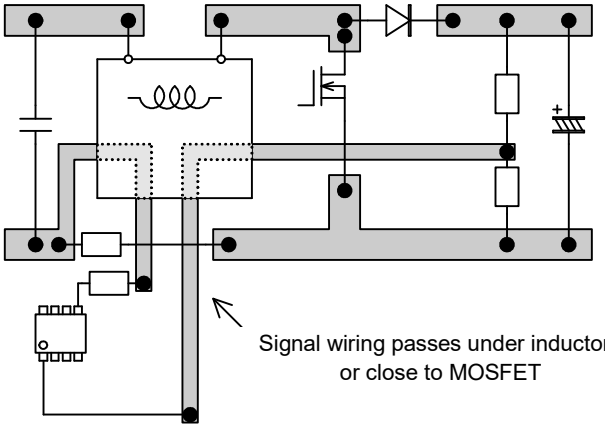


Fig.34 Example of inadvisable pattern

(2) Typical GND wiring in IC area

To minimize influences on IC of noises from main circuit, separate GND of IC and signal lines for parts of IC area, and GND of PFC main circuit away from each other, and connect them via one point near current detecting resistance Rs and output capacitance.
IS signal whose voltage level is low is liable to noise. Minimize lengths of IS pin-Rs and Rs-GND wiring.
Arrange VCC-GND capacitance close to IC. Otherwise, the effect will be poor.
Arrange the capacitance between IC area input terminal and GND close to IC. It also has a function of noise elimination and, if away from IC, it will be affected by noise.

Caution:
Wiring is exemplified for you to understand how to connect the GND line.
Noise and incidental erratic operations differ from one instrument to another. Adopting any wiring exemplified in Fig. 35 will not necessarily guarantee normal operations of your instruments.

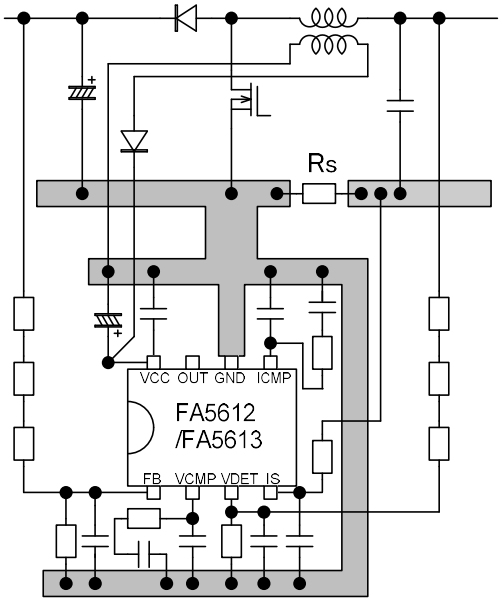


Fig.35 Example of advisable GND wiring

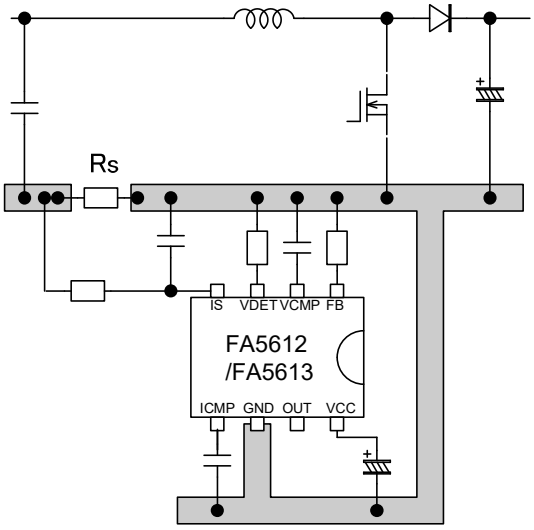


Fig.36 Example of inadvisable GND wiring

(GND is common to signal line parts and main circuit)

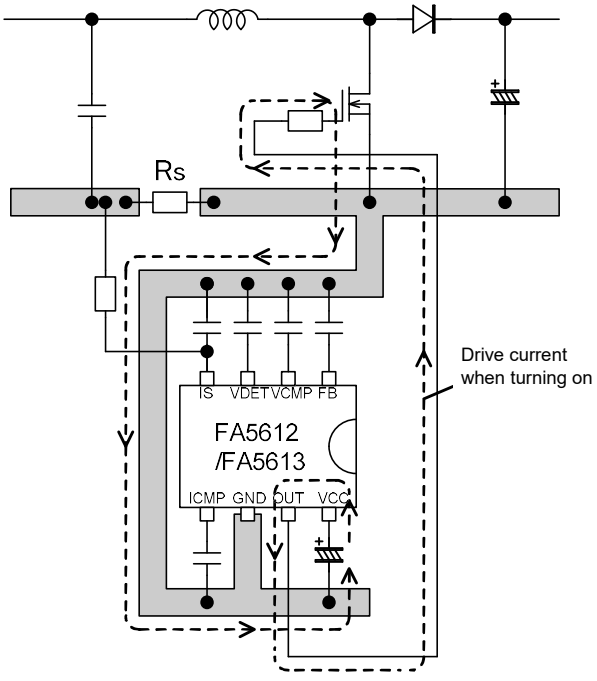


Fig.37 Example of inadvisable GND wiring

(Liable to noise when turning on if GND is

common to VCC capacitance and signal line)

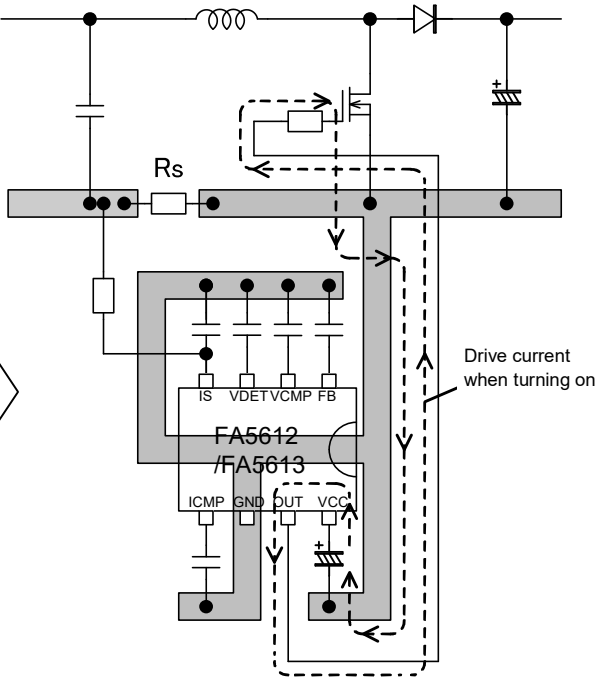


Fig.38 Example of GND wiring

(GND of VCC capacitance is

distinct from signal line GND)

(3) Precautions in use regarding terminal noise

If noise is applied to any IC pin, an erratic operation may be caused. Proceed to design upon respecting the precautions below.

Condition	Pin	Malfunction in fear	Input regulations	Cautions in design
Input noise (within absolute maximum ratings)	FB	switching may stop when noise is over over voltage protection level	input signal is only for feedback voltage of output voltage	connect condenser near terminal pin
		IC may become stanbay mode when noise is under short detection level		
		offset occurs in output voltage and output voltage rises or falls		
	VCMP	output of multiplier output becomes unstable, and input current waveform may disturbed	cancel noise	confirm sufficiently phase compensation constant
		switching may become when noise is over threshold voltage		
		switching may stop when noise is under threshold voltage		
	VDET	output of multiplier output becomes unstable, and input current waveform may be disturbed	cancel noise	connect condensor near pin
	IS	current may be detected incorrectly	cancel noise	connect condensor near pin
		It may turn off when noise is over overcurrent protection level		
	ICMP	because a duty changes, input current waveform may be disturbed	cancel noise	confirm sufficiently phase compensation constant
	GND	reference voltage changes, IC may not behave normally	cancel noise	ground wiring should be a wide wiring
	OUT	the output may fall not to be able to drive Mos normally when signals more than the ability of the driver are input	cancel noise	-
	VCC	IC may stop when noise under UVLO is input	don't input noise under UVLO when moving	connect condensor near pin
Input minus voltage (less than absolute maximum voltage)	FB	a parasitism element works, and the malfunction such as IC stop may occur	don't input minus voltage less than maximum absolute voltage	-
	VCMP			
	VDET			
	ICMP			
	VCC			
	IS	IC may be destroyed		
	OUT	IC may be destroyed		
	VCC	a parasitism element works, and the malfunction such as IC stop may occur		
Input plus voltage (more than absolute maximum voltage)	FB	IC may be destroyed	don't input minus voltage more than maximum absolute voltage	-
	VCMP			
	VDET			
	ICMP			
	IS	gnd level may be changed		
	OUT	IC may be destroyed		
	VCC			

13. Example of application circuit (390V / 1.5A output)

