Complementary Power Transistors

DPAK for Surface Mount Applications

MJD2955 (PNP), MJD3055 (NPN)

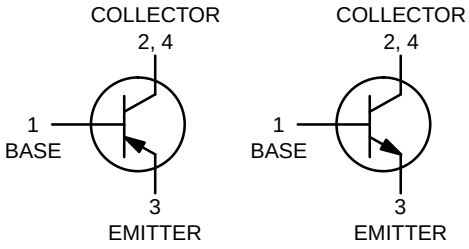
SILICON
POWER TRANSISTORS
10 AMPERES
60 VOLTS, 20 WATTS

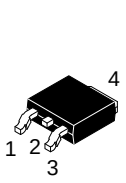
Designed for general purpose amplifier and low speed switching applications.

Features

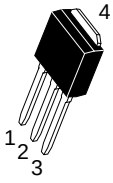
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Electrically Similar to MJE2955 and MJE3055
- High Current Gain-Bandwidth Product
- Epoxy Meets UL 94 V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

COMPLEMENTARY





DPAK
CASE 369C
STYLE 1



IPAK
CASE 369D
STYLE 1

MAXIMUM RATINGS

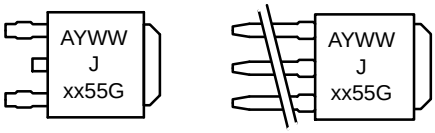
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ T_C = 25 °C Derate above 25 °C	P_D†	 20 0.16	 W W/°C
Total Power Dissipation (Note 1) @ T_A = 25 °C Derate above 25 °C	P_D	 1.75 0.014	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

† Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

MARKING DIAGRAMS



DPAK IPAK

A = Assembly Location
Y = Year
WW = Work Week
Jxx55 = Device Code
x = 29 or 30
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	71.4	°C/W

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	50	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150 °C)	I_{CEX}	– –	0.02 2	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150 °C)	I_{CBO}	– –	0.02 2	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	100 –	–
Collector-Emitter Saturation Voltage (Note 3) (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8	Vdc
Base-Emitter On Voltage (Note 3) (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2	–	MHz

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL CHARACTERISTICS

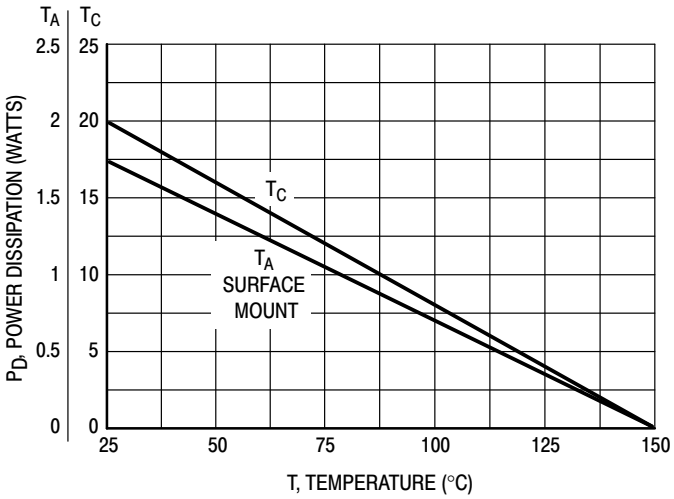

Figure 1. Power Derating

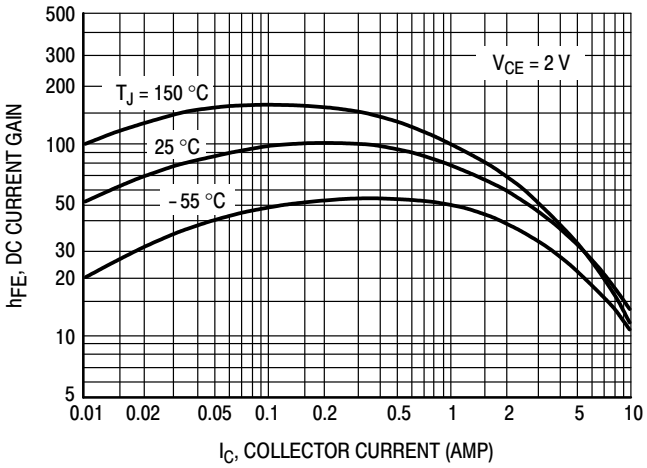

Figure 2. DC Current Gain

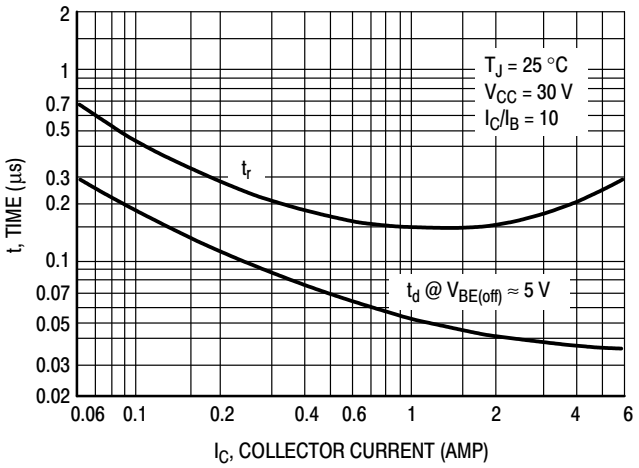

Figure 3. Turn-On Time

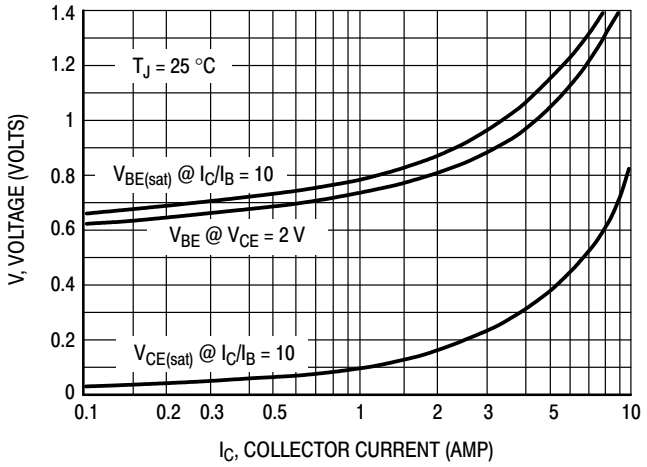

Figure 4. “On” Voltages, MJD3055

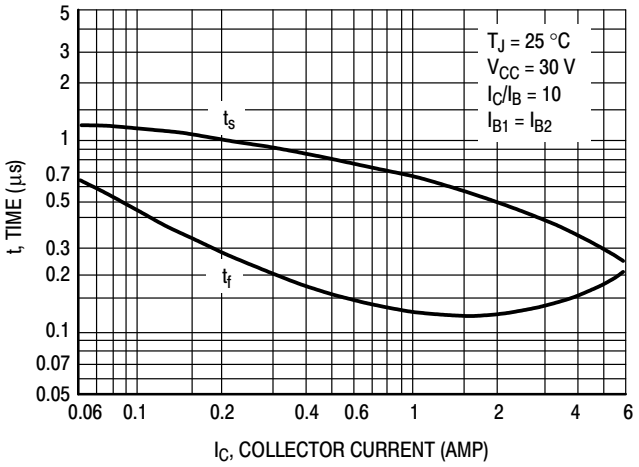

Figure 5. Turn-Off Time

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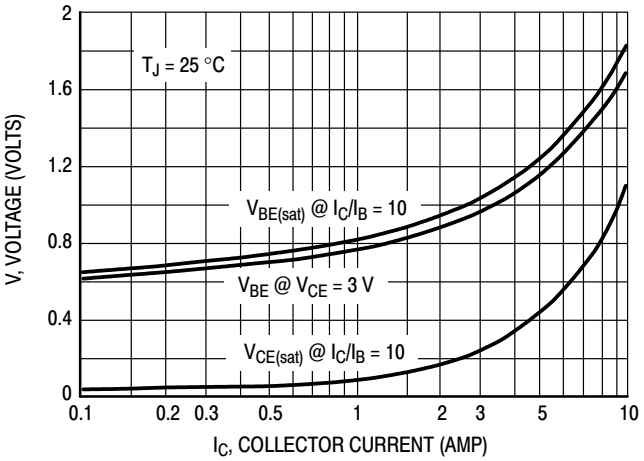

Figure 6. “On” Voltages, MJD2955

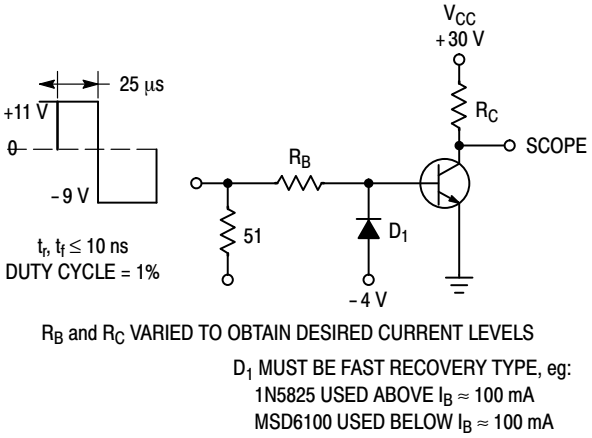

Figure 7. Switching Time Test Circuit

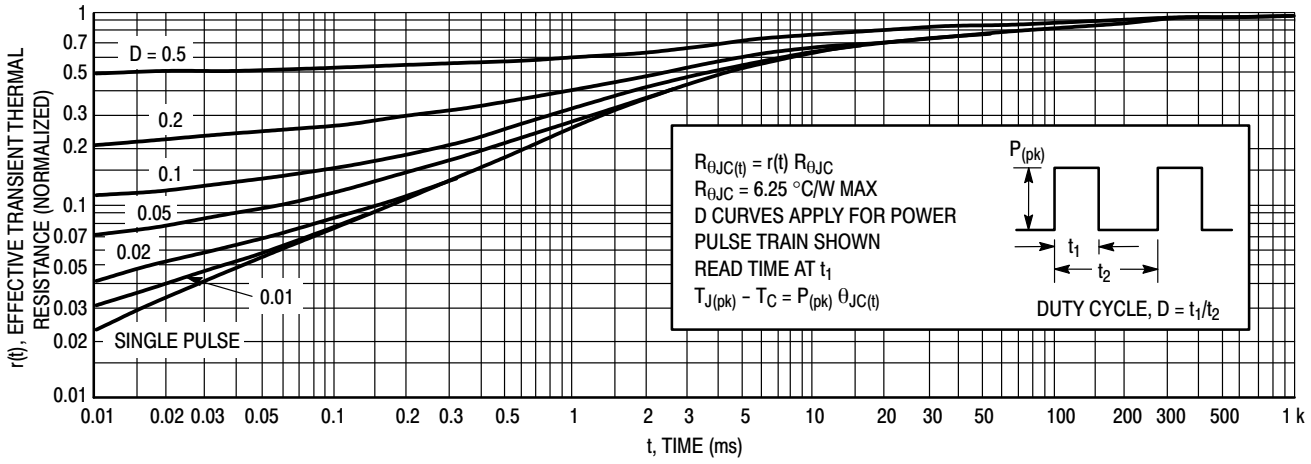

Figure 8. Thermal Response

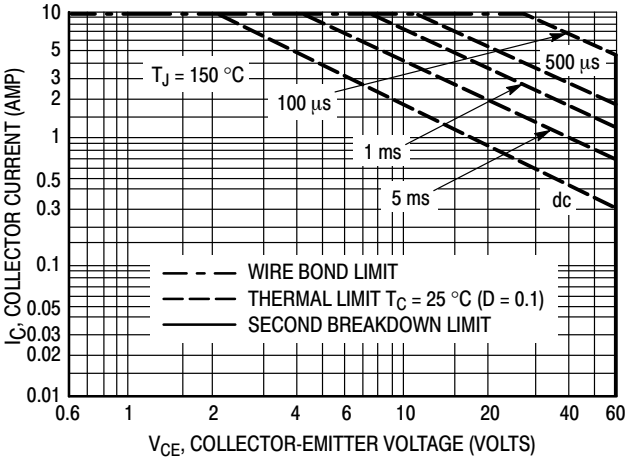

Figure 9. Maximum Forward Bias Safe Operating Area

Forward Bias Safe Operating Area Information

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150$ °C. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD2955G	DPAK (Pb-Free)	369C	75 Units / Rail
MJD2955T4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD2955T4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
MJD3055T4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD3055T4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel

DISCONTINUED (Note 4)

MJD2955-1G	IPAK (Pb-Free)	369D	75 Units / Rail
MJD3055G	DPAK (Pb-Free)	369C	75 Units / Rail

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

4. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
14	Rebranded the document to **onsemi** format. MJD2955-1G, MJD3055G OPNs marked as Discontinued.	4/1/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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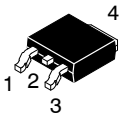
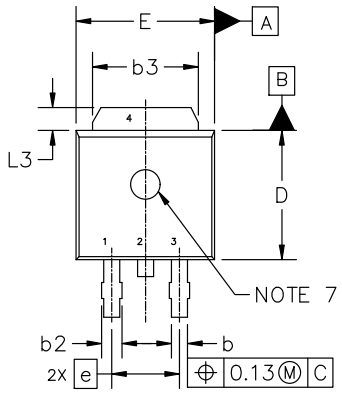


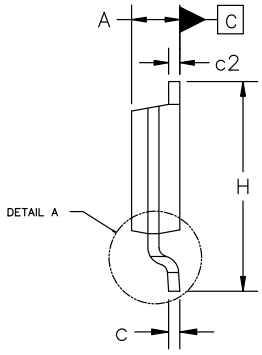
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

SCALE 1:1

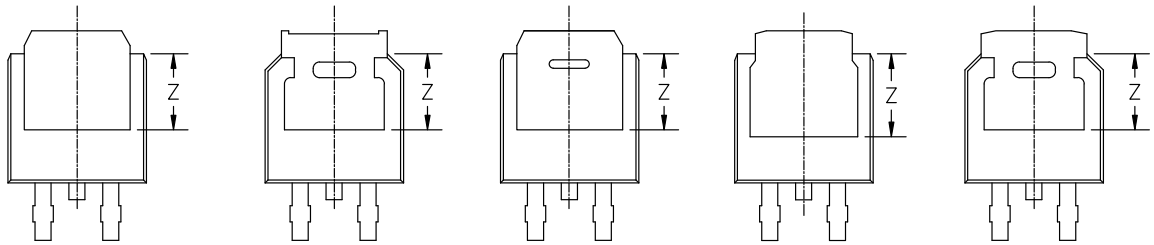


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−

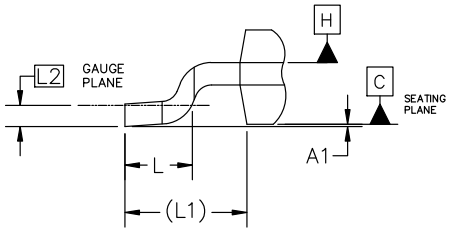


BOTTOM VIEW

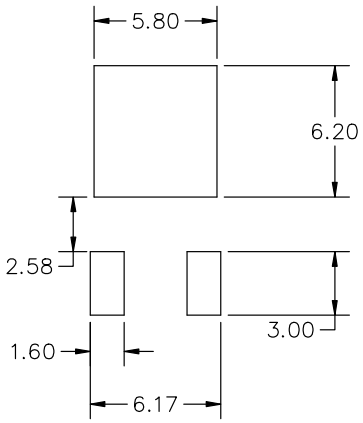
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

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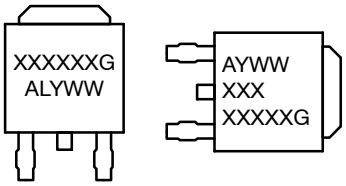
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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