UCCx808-x Low Power Current Mode Push-Pull PWM

1 Features

- Dual output drive stages in push-pull configuration
- 130μA typical starting current
- 1mA typical run current
- Operation to 1MHz
- Internal soft-start
- On-chip error amplifier with 2MHz gain bandwidth product
- On-chip VDD clamping
- Output drive stages capable of 500mA peak source current, 1A peak sink current

2 Applications

- Server and desktop power supplies
- Telecom power supplies
- DC-DC converters
- Switched-mode power supplies

3 Description

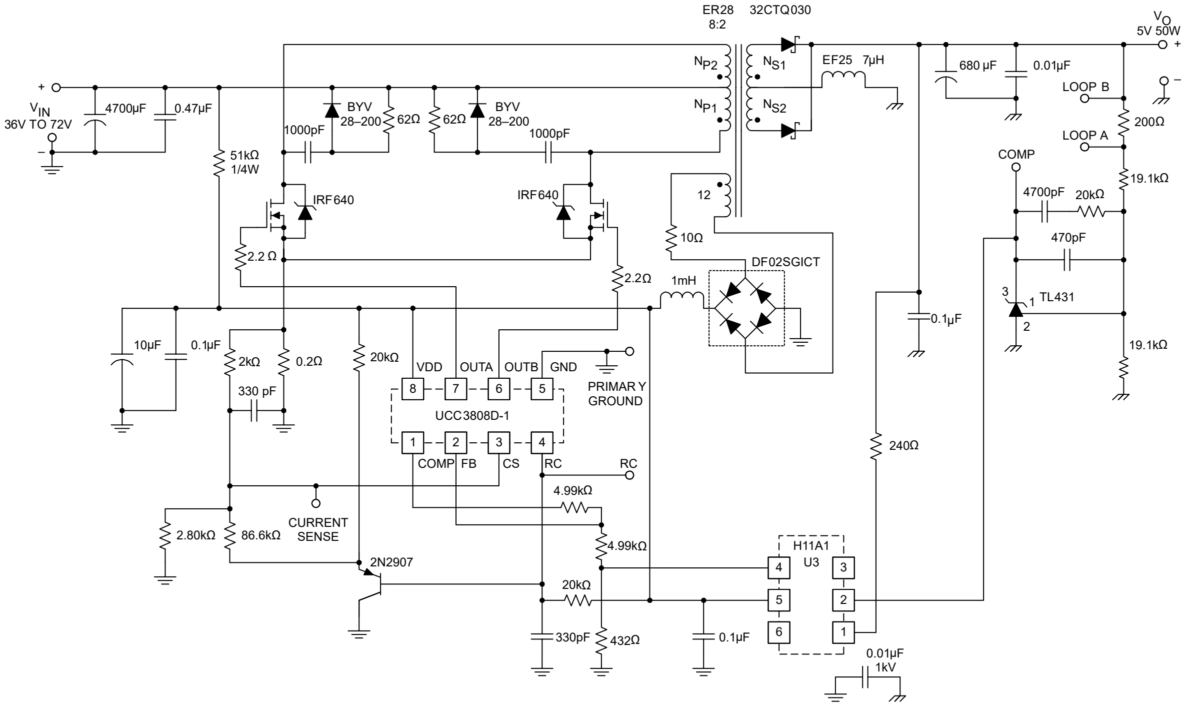
The UCCx808-x is a family of BiCMOS push-pull pulse-width modulators that are high-speed and low-power. The UCCx808 contains all of the control and drive circuitry required for offline or DC-to-DC fixed frequency current-mode switching power supplies with a minimal external parts count.

The UCCx808-x dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns, depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
UCC2808-1	D (SOIC, 8)	4.90mm × 6.00mm
UCC2808-2		
UCC3808-1		
UCC3808-2		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

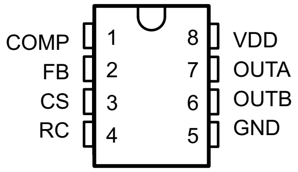


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Output of the error amplifier and the input of the PWM comparator.
CS	3	I	Input to the PWM, peak current, and overcurrent comparators.
FB	2	I	Inverting input to the error amplifier.
GND	5	—	Reference ground and power ground for all functions.
OUTA	7	O	Alternating high current output stage.
OUTB	6	O	Alternating high current output stage.
RC	4	I	Oscillator programming pin.
VDD	8	—	Power input connection for this device.

(1) I=Input; O=Output; I/O= Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage (IDD ≤ 10mA)		15	V
	Supply current		20	mA
	OUTA/OUTB source current (peak)(2)	–0.5		A
	OUTA/OUTB sink current (peak)(2)		1	A
	Analog inputs (FB, CS) – 0.3V to VDD + 0.3V		6	V
	Power dissipation at T A = 25°C (D Package)		650	mW
T_J	Junction temperature	–55	150	°C
	Lead temperature (soldering, 10 seconds)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Currents are positive into, negative out of the specified terminal. Consult the Packaging Section of the *Power Supply Control Data Book* for thermal limitations and considerations of packages.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply Voltage	UCCx808-1	13	14	V
		UCCx808-2	5	14	
T_J	Junction Temperature	UCC2808-x	–40	85	°C
		UCC3808-x	0	70	

5.4 Thermal Information

THERMAL METRIC(1)		UCCx808	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3808-x, –40°C to 85°C for the UCC2808-x and –55°C to 125°C for the UCC1808-x, VDD = 10V(1), 1µF capacitor from VDD to GND, R = 22kΩ, C = 330pF, T_A = T_J, (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR SECTION					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD(2)		0.44	0.5	0.56	V/V
ERROR AMPLIFIER SECTION					
Input voltage	COMP = 2V	1.95	2	2.05	V
Input bias current		–1		1	µ A
Open-loop voltage gain		60	80		dB
COMP sink current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
COMP source current	FB = 1.3V, COMP = 3.5V	–0.25	–0.5		mA
PWM SECTION					
Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
Minimum duty cycle	COMP =0V			0%	
CURRENT SENSE SECTION					
Gain(3)		1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5V(4)	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5V, CS from 0mV to 600mV		100	200	ns
CS source current		–200			nA
Over current threshold		0.7	0.75	0.8	V
COMP to CS offset	CS = 0V	0.35	0.8	1.2	V
OUTPUT SECTION					
OUT low level	I = 100mA		0.5	1	V
OUT high level	I = – 50mA, VDD – OUT		0.5	1	V
Rise time	C_L =1nF		25	60	ns
Fall time	C_L = 1nF		25	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start threshold	UCCx808-1(1)	11.5	12.5	13.5	V
	UCCx808-2	4.1	4.3	4.5	
Minimum operating voltage after start	UCCx808-1	7.6	8.3	9	V
	UCCx808-2	3.9	4.1	4.3	
Hysteresis	UCCx808-1	3.5	4.2	5.1	V
	UCCx808-2	0.1	0.2	0.3	
SOFT-START SECTION					
COMP rise time	FB = 1.8V, rise from 0.5V to4V		3.5	20	ms
OVERALL SECTION					
Start-up current	VDD < start threshold		130	260	µA
Operating supply current	FB = 0V, CS = 0V (5) (1)		1	2	mA
VDD zener shunt voltage	IDD = 10mA(6)	13	14	15	V

(1) Does not include current in the external oscillator network.
(2) Measured at RC. Signal amplitude tracks VDD.
(3) Gain is defined by: Equation 1
(4) Parameter measured at trip point of latch with FB at 0V.
(5) For UCCx808 – 1, set VDD above the start threshold before setting at 10V
(6) Start threshold and Zener shunt threshold track one another.

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}, 0 \le V_{CS} \le 0.4V \tag{1}$$

5.6 Typical Characteristics

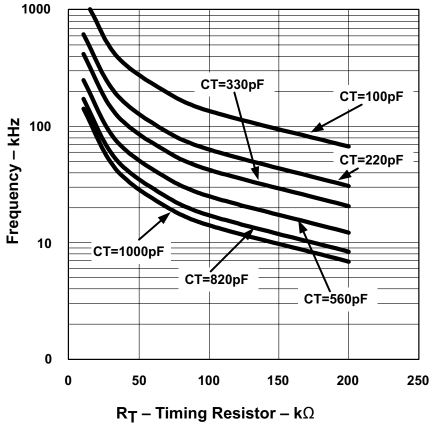


Figure 5-1. Frequency vs Timing Resistor

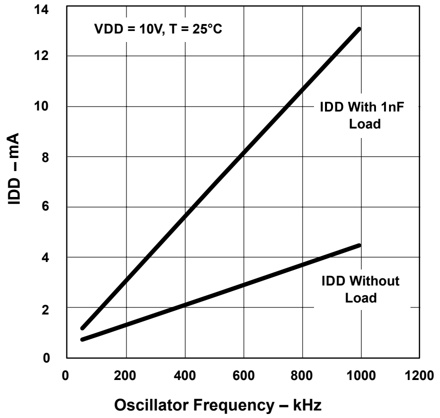


Figure 5-2. IDD vs Oscillator Frequency

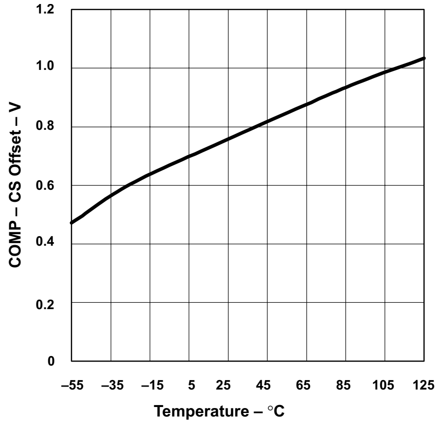


Figure 5-3. CS Offset vs Temperature

6 Detailed Description

6.1 Overview

The UCCx808-x device is a highly-integrated push-pull PWM controller that is low power and has a current mode. The controller employs low starting current and an internal control algorithm that offers accurate static output voltage regulation against line and load. The UCCx808-x family offers a variety of package temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for offline and battery-powered system.

Table 6-1. Undervoltage Lockout Levels

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCx808-1	12.5V	8.3V
UCCx808-2	4.3V	4.1V

Table 6-2. Undervoltage Lockout Options

$T_A = T_J$	PACKAGED DEVICES	
	UVLO OPTION	SOIC (D)
–40°C to 85°C	12.5V / 8.3V	UCC2808D-1
	4.3V / 4.1V	UCC2808D-2
0°C to 70°C	12.5V / 8.3V	UCC3808D-1
	4.3V / 4.1V	UCC3808D-2

6.2 Functional Block Diagram

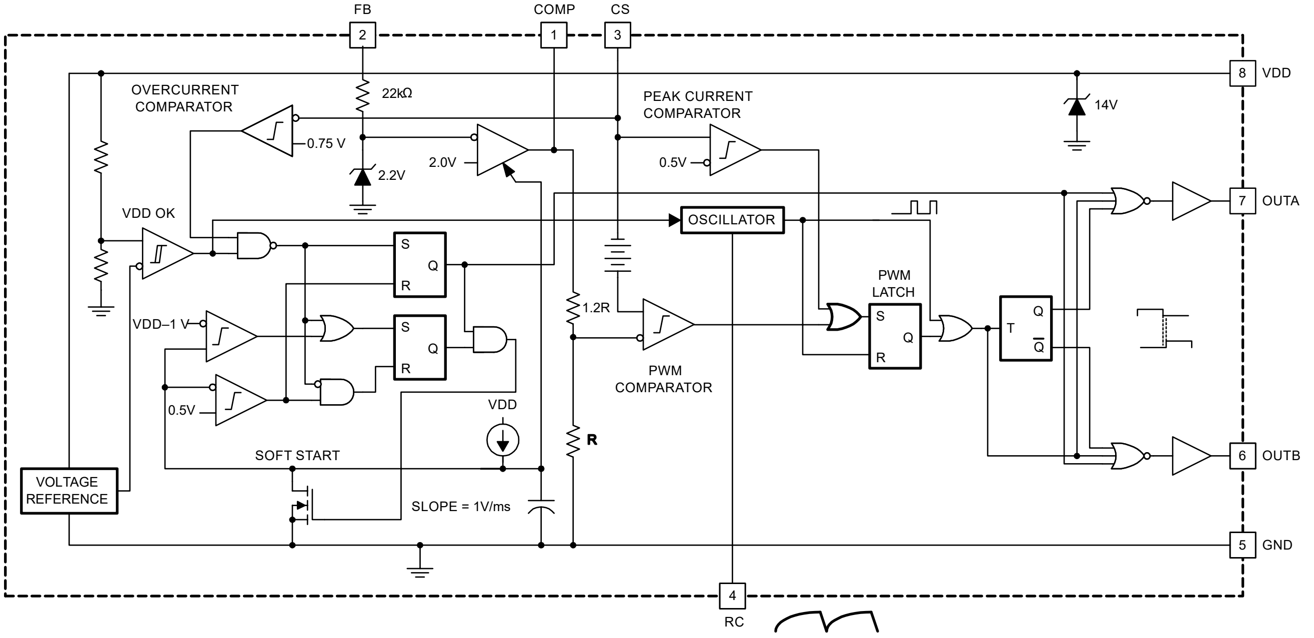
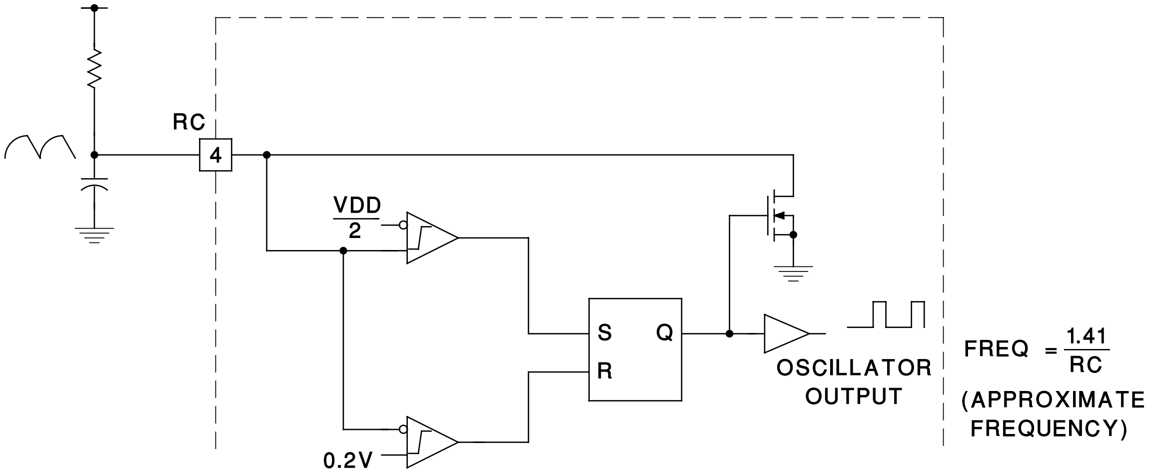


Figure 6-1. Functional Block Diagram



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch at ½ the oscillator frequency, with duty cycle of <50% for both outputs.

Figure 6-2. Block Diagram for Oscillator

6.3 Feature Description

6.3.1 Pin Descriptions

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin sources and sinks current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft-start. Soft-start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC3808, a low-impedance printed-circuit-board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. Dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. Tn many cases, external Schottky clamp diodes are not required.

RC: The oscillator programming pin. The oscillator of the UCC3808-x tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 6-2 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula:

$$f_{\mathrm{OSCILLATOR}} = \frac{1.41}{\mathrm{RC}} \tag{2}$$

where

- Frequency is in hertz (Hz)
- Resistance is in Ω
- Capacitance is in farads (F)

The recommended range of timing resistors is between 10kΩ and 200kΩ and range of timing capacitors is between 100pF and 1000pF. Avoid timing resistors less than 10kΩ.

For best performance, keep the timing capacitor lead to GND, timing resistor lead from VDD, and leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$$f_{\mathrm{OSCILLATOR}} = \frac{1.41}{\mathrm{RC}} \tag{3}$$

where

- F is frequency

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor.

A 1µF decoupling capacitor is recommended.

6.4 Device Functional Modes

6.4.1 VCC

When VCC becomes above 12.5V (for UCCx808-1) or 4.3V (for UCCx808-2), the device is enable, and after all fault conditions are cleared, the gate driver starts with soft-start. When VCC drops below 8.3V (for UCCx808-1) or 4.1V (for UCCx808-2), the device enters the UVLO protection mode and both gate drivers are actively pulled low.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UCCx808-x PWM controller contains all of the features needed to implement push-pull topology, using current-mode control in a small 8-pin package. The UCCx808-x is designed for current-mode control push-pull topology. UCCx808-x employs advantages of current-mode control, peak current sense, overcurrent protection.

7.2 Typical Application

A 200kHz push-pull application circuit with a full wave rectifier is shown in Figure 7-1.

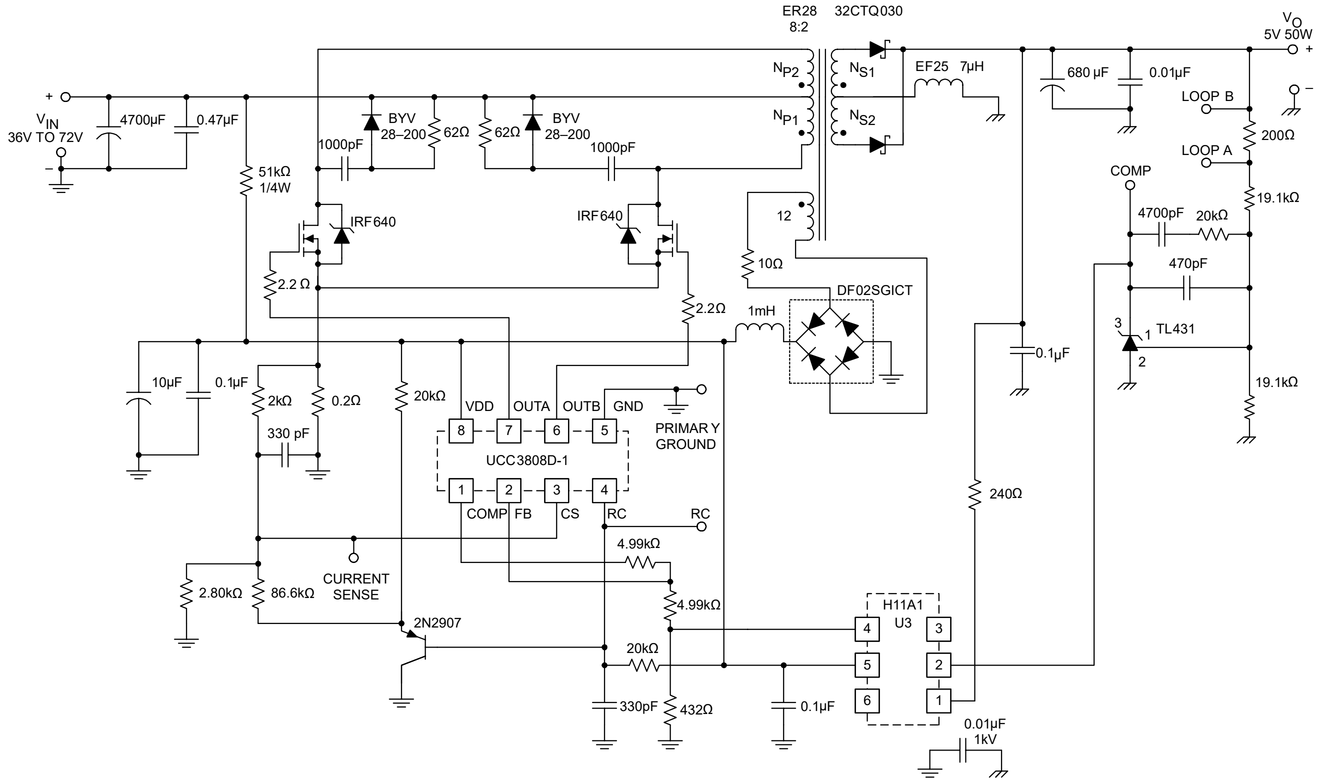


Figure 7-1. Typical Application Diagram: 48V In, 5V, 50W Output

7.2.1 Design Requirements

Table 7-1 lists the design parameters of the UCC3808-x.

Table 7-1. Design Parameters

DESIGN PARAMETER	TARGET VALUE
Output voltage	5V
Rated output power	50W
Input DC voltage range	36V to 72V
Switching frequency	210kHz

7.2.2 Detailed Design Procedure

The output, VO, provides 5V at 75W maximum and is electrically isolated from the input. Because the UCC3808 is a peak current mode controller, the 2N2222A emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1µF is suggested for placement as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady-state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the UC3965 Precision Reference with Low Offset Error Amplifier. Small signal compensation with tight voltage regulation is achieved using the UC3965 device part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown in Figure 7-1. The main power transformer is a low profile design, EFD size 25, using Magnetics® Inc. P material which is a good choice at the frequency and temperature in Design Parameters. The input voltage ranges from 36V DC to 72V DC.

7.2.3 Application Curves

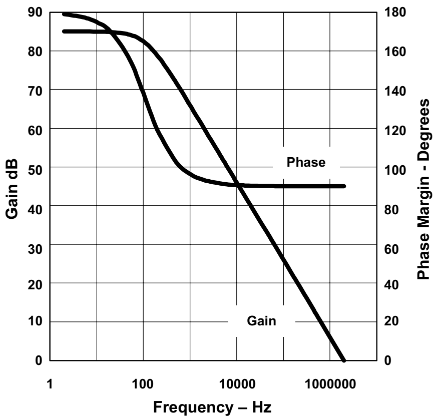


Figure 7-2. Error Amplifier Gain and Phase Response vs Frequency

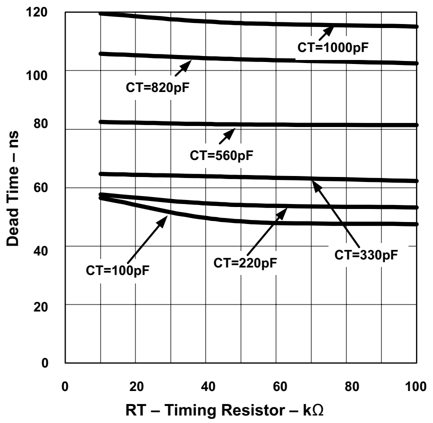


Figure 7-3. Dead Time vs Timing Resistor

7.3 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor, because UCCx808-x is a controller with a 1A driver capability. The UCCx808-x device requires the placement of low-ESR noise-decoupling capacitance as directly as possible from the VDD terminal to the GND terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. The recommended electrolytic capacitor is a 10µF or 25V capacitor.

The recommended decoupling capacitors are a 0.1µF 0603-sized 25V X7R capacitor.

7.4 Layout

7.4.1 Layout Guidelines

- Place the VDD capacitor as close as possible between the VDD terminal and GND of the UCCx808-x, tracked directly to both terminals.
- A small, external filter capacitor is recommended on the CS terminal. Track the filter capacitor as directly as possible from the CS to GND terminal.
- The tracking and layout of the FB terminal and connecting components is critical to minimize noise pick-up and interference in the magnetic sensing block. Minimize the total surface area of trances on the FB net.
- The OUTA/OUTB terminal has high internal sink or source current capability. An external gate resistor is recommended. The value depends on the choice of power MOSFET, efficiency and EMI considerations. A

pulldown resistor on the gate of the external MOSFET is recommended to prevent the MOSFET gate from floating on if there is an open-circuit error in the gate drive path.

7.4.2 Layout Example

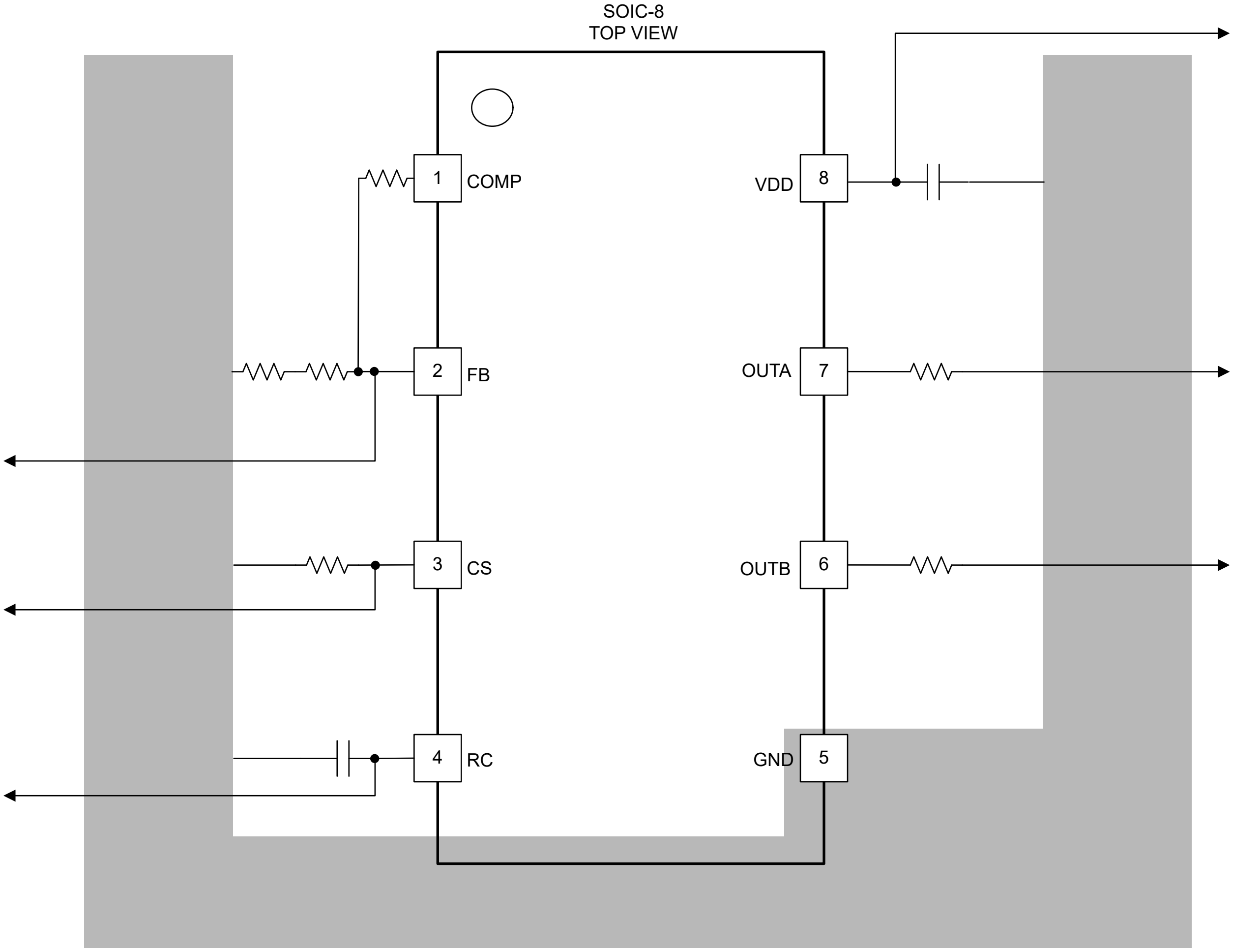


Figure 7-4. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Texas Instruments *Unitrode Power Supply Control Products (PS)* data book

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC2808-1	Click here	Click here	Click here	Click here	Click here
UCC2808-2	Click here	Click here	Click here	Click here	Click here
UCC3808-1	Click here	Click here	Click here	Click here	Click here
UCC3808-2	Click here	Click here	Click here	Click here	Click here

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2015) to Revision F (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Deleted PDIP packaging information throughout the document	1
• Deleted TSSOP packaging information	4
• Added *Thermal Information* table	4

Changes from Revision D (August 2002) to Revision E (April 2015)	Page
• Removed references to the TSSOP packaging	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2808D-1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2808-1
UCC2808D-2	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2808-2
UCC2808DTR-1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-1
UCC2808DTR-1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC2808DTR-1	2808-1
UCC2808DTR-2	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-2
UCC2808DTR-2.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC2808DTR-2	2808-2
UCC2808DTR-2G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-2
UCC3808D-1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3808-1
UCC3808D-2	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3808-2
UCC3808DTR-1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(3808-1, UCC3808) D-1
UCC3808DTR-1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC3808DTR-1	(3808-1, UCC3808) D-1
UCC3808DTR-2	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808-2
UCC3808DTR-2.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC3808DTR-2	3808-2
UCC3808DTR-2G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808-2
UCC3808N-1	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 70	UCC3808N-1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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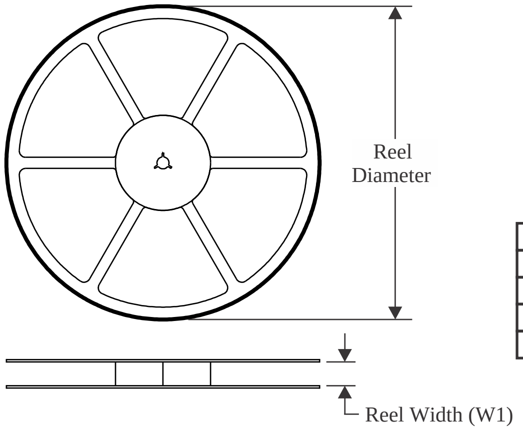
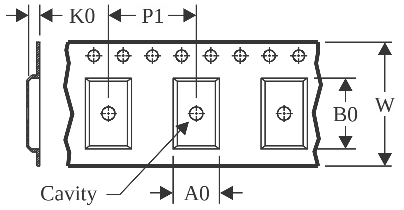
TAPE AND REEL INFORMATION

REEL DIMENSIONS

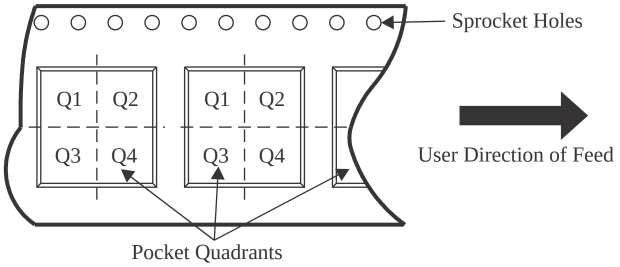


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

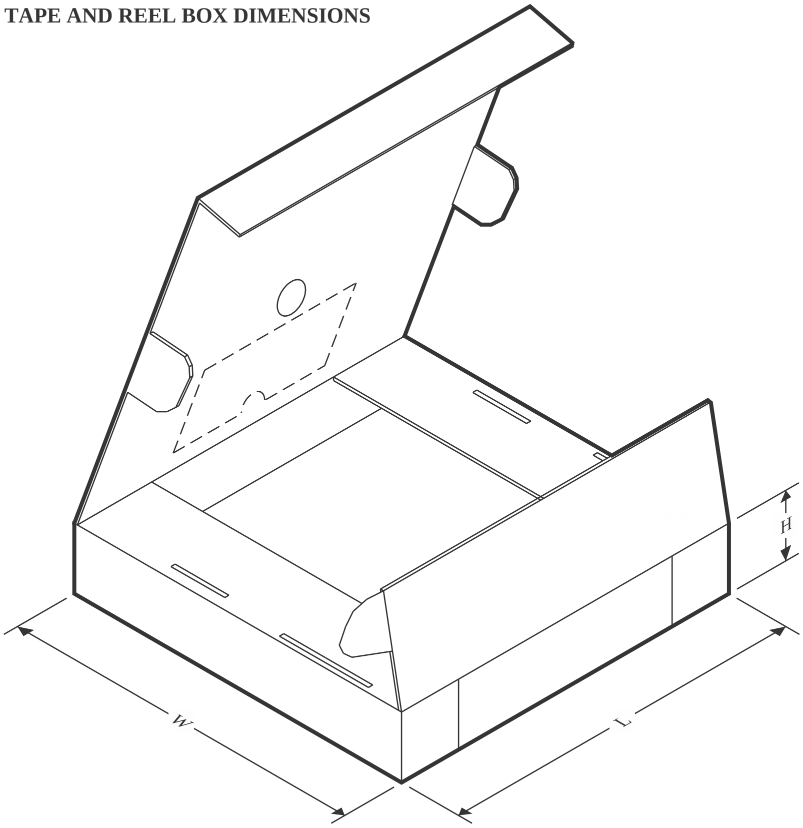
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



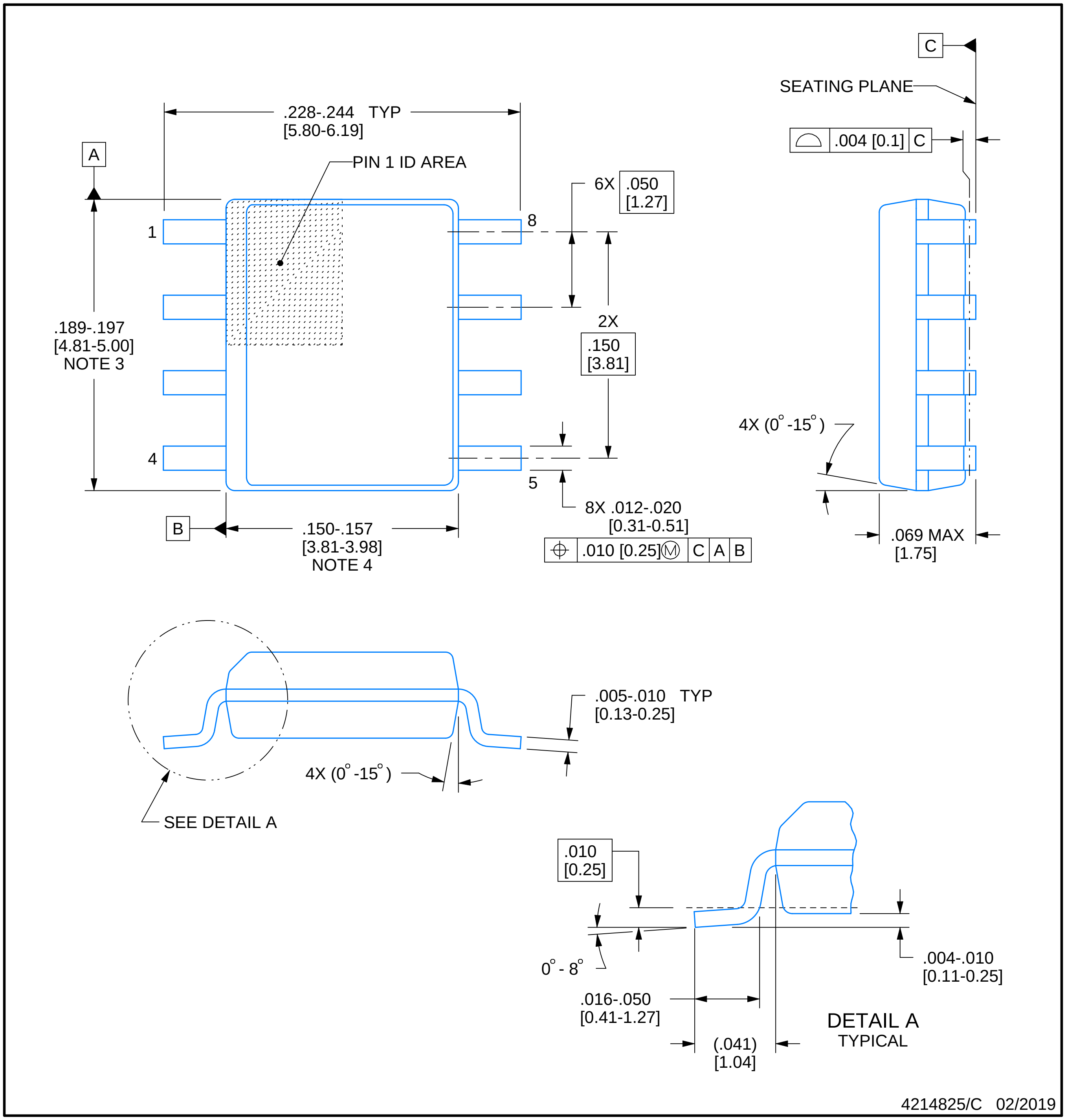
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808DTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC2808DTR-2	SOIC	D	8	2500	353.0	353.0	32.0
UCC3808DTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC3808DTR-2	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

SOIC - 1.75 mm max height

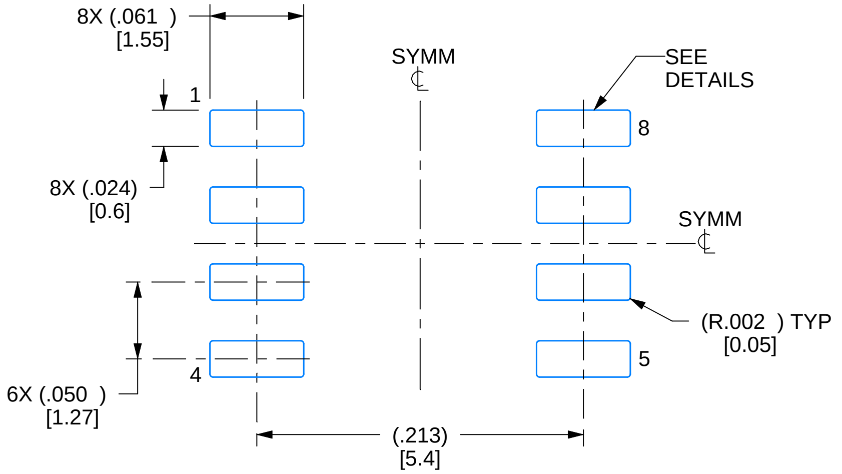
SMALL OUTLINE INTEGRATED CIRCUIT



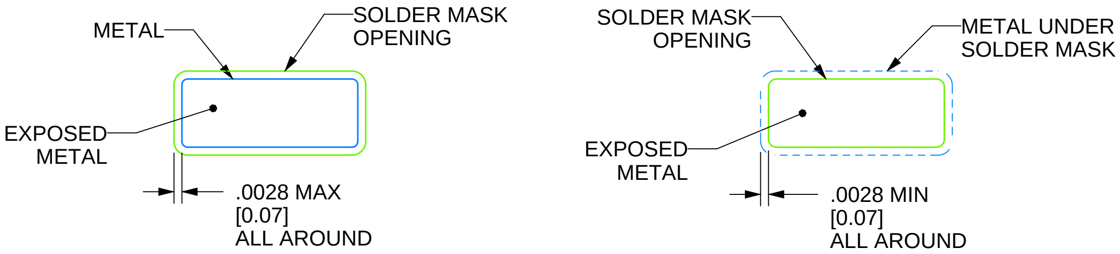
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



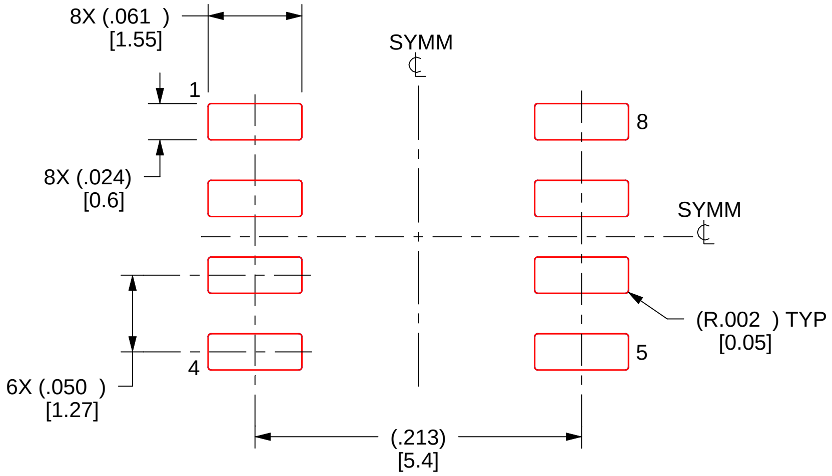
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

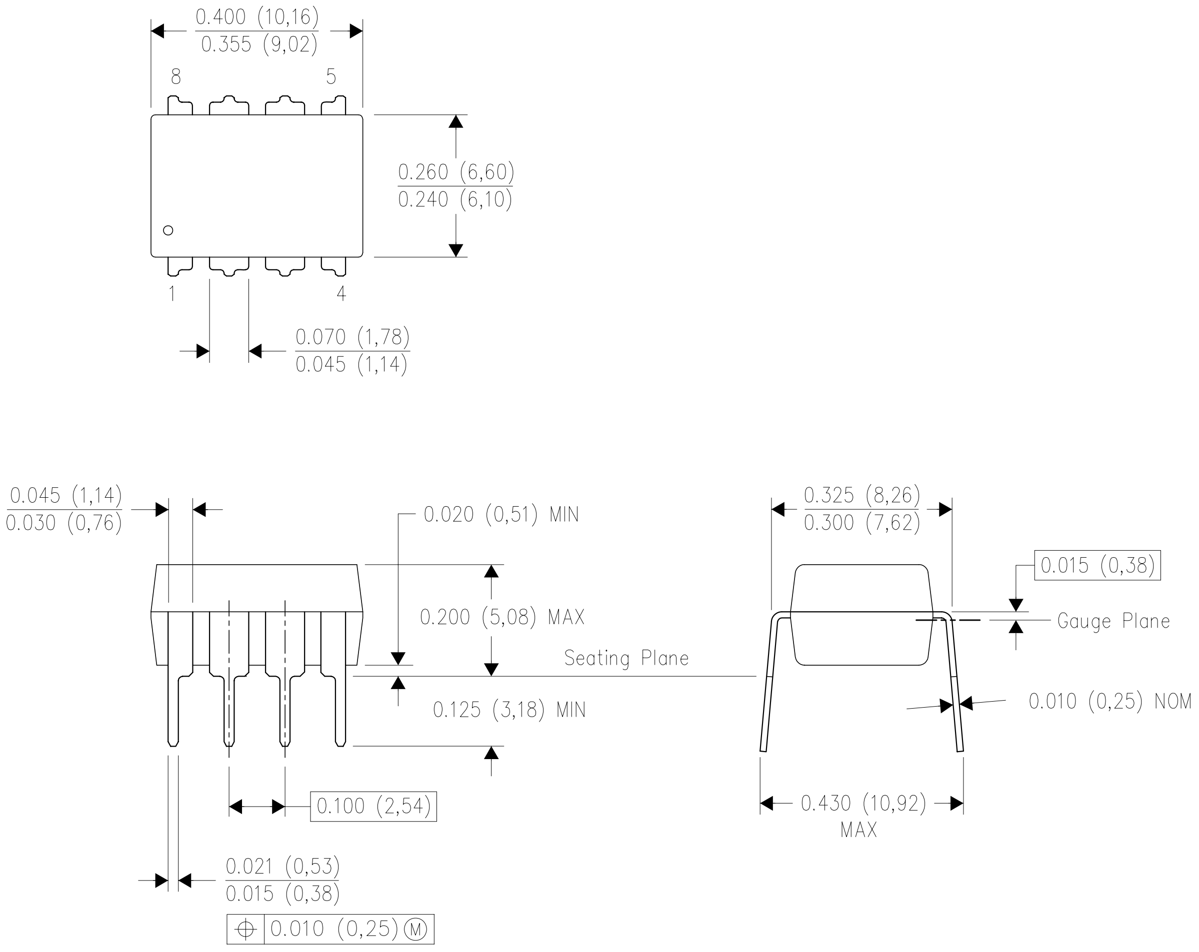


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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