Description

The M16C/62A group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office, communications, industrial equipment, and other high-speed processing applications.

The M16C/62A group includes a wide range of products with different internal memory types and sizes and various package types.

Features

- Memory capacity ..... ROM (See Figure 1.1.4. ROM Expansion)
  RAM 3K to 20K bytes
- Shortest instruction execution time ..... 62.5ns (f(XIN)=16MHz, VCC=5V)
  100ns (f(XIN)=10MHz, VCC=3V, with software one-wait) : Mask ROM, flash memory 5V version
- Supply voltage ..... 4.2V to 5.5V (f(XIN)=16MHz, without software wait) : Mask ROM, flash memory 5V version
  2.7V to 5.5V (f(XIN)=10MHz with software one-wait) : Mask ROM, flash memory 5V version
- Low power consumption ..... 25.5mW (f(XIN)=10MHz, with software one-wait, VCC = 3V)
- Interrupts ..... 25 internal and 8 external interrupt sources, 4 software interrupt sources; 7 levels (including key input interrupt)
- Multifunction 16-bit timer ..... 5 output timers + 6 input timers
- Serial I/O ..... 5 channels (3 for UART or clock synchronous, 2 for clock synchronous)
- DMAC ..... 2 channels (trigger: 24 sources)
- A-D converter ..... 10 bits X 8 channels (Expandable up to 10 channels)
- D-A converter ..... 8 bits X 2 channels
- CRC calculation circuit ..... 1 circuit
- Watchdog timer ..... 1 line
- Programmable I/O ..... 87 lines
- Input port ..... 1 line (P85 shared with $\overline{\text{NMI}}$ pin)
- Memory expansion ..... Available (to a maximum of 1M bytes)
- Chip select output ..... 4 lines
- Clock generating circuit ..... 2 built-in clock generation circuits
  (built-in feedback resistor, and external ceramic or quartz oscillator)

Applications

Audio, cameras, office equipment, communications equipment, portable equipment

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Pin Configuration

Figures 1.1.1 and 1.1.2 show the pin configurations (top view).

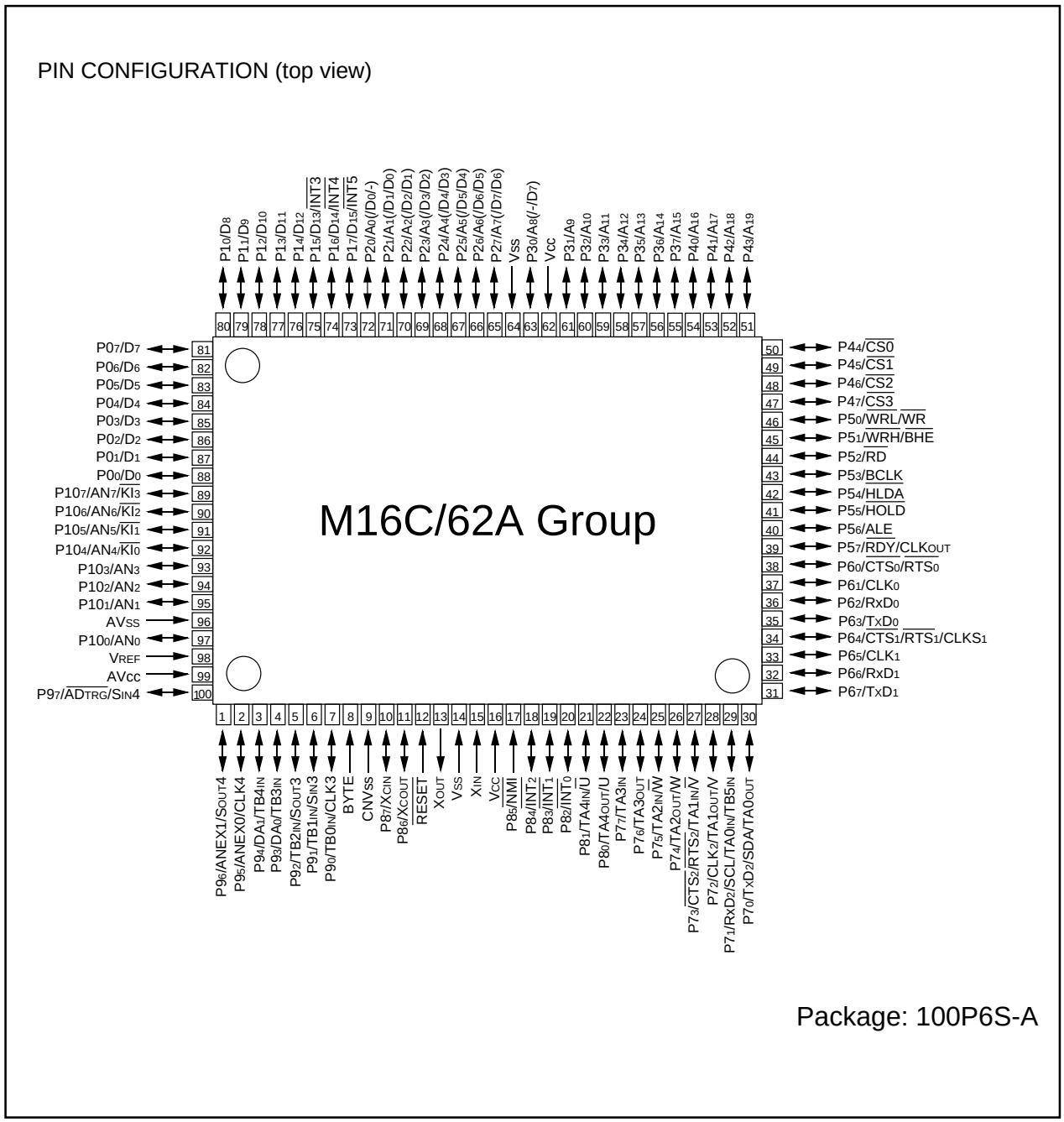


Figure 1.1.1. Pin configuration (top view)

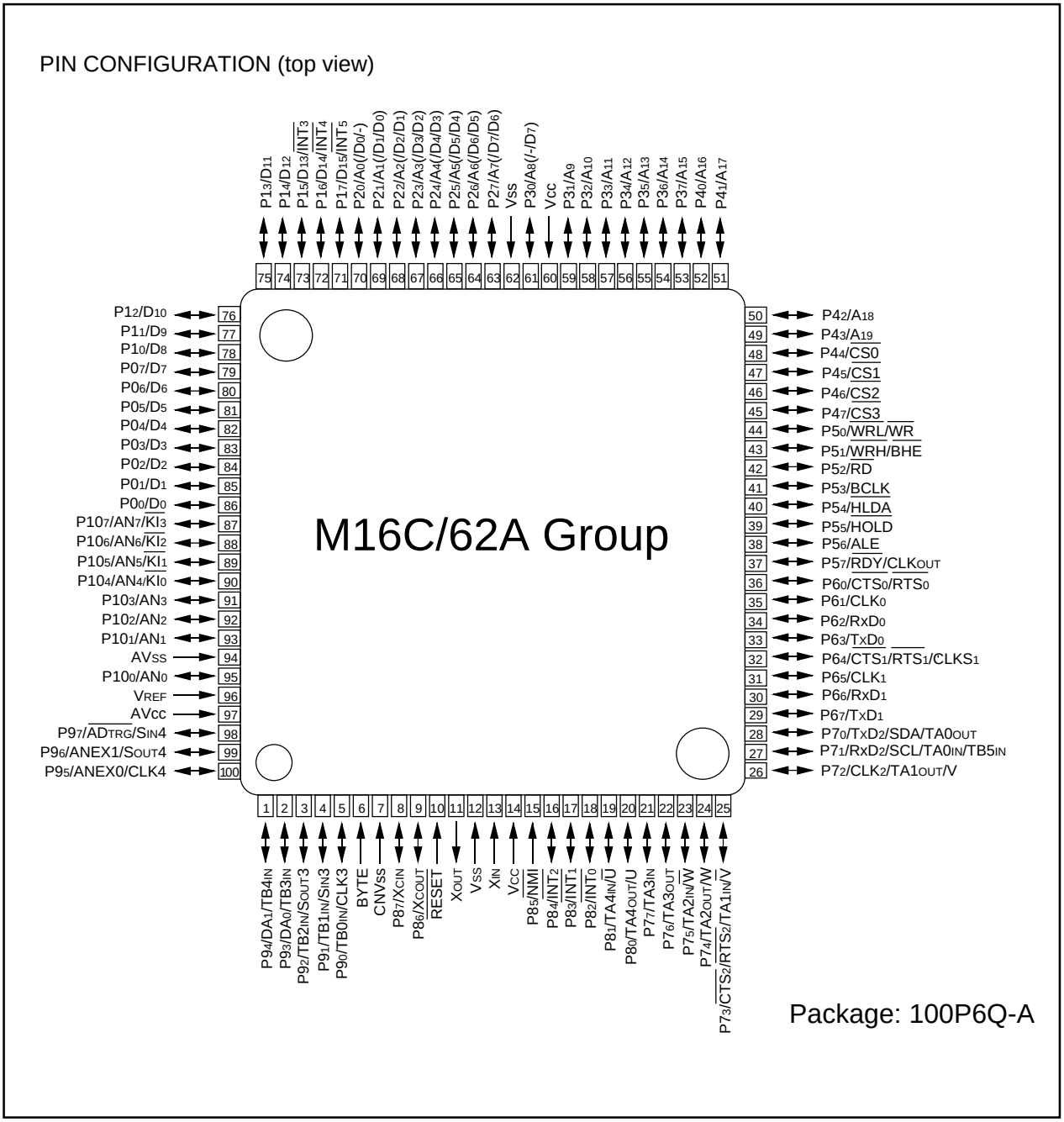


Figure 1.1.2. Pin configuration (top view)

Block Diagram

Figure 1.1.3 is a block diagram of the M16C/62A group.

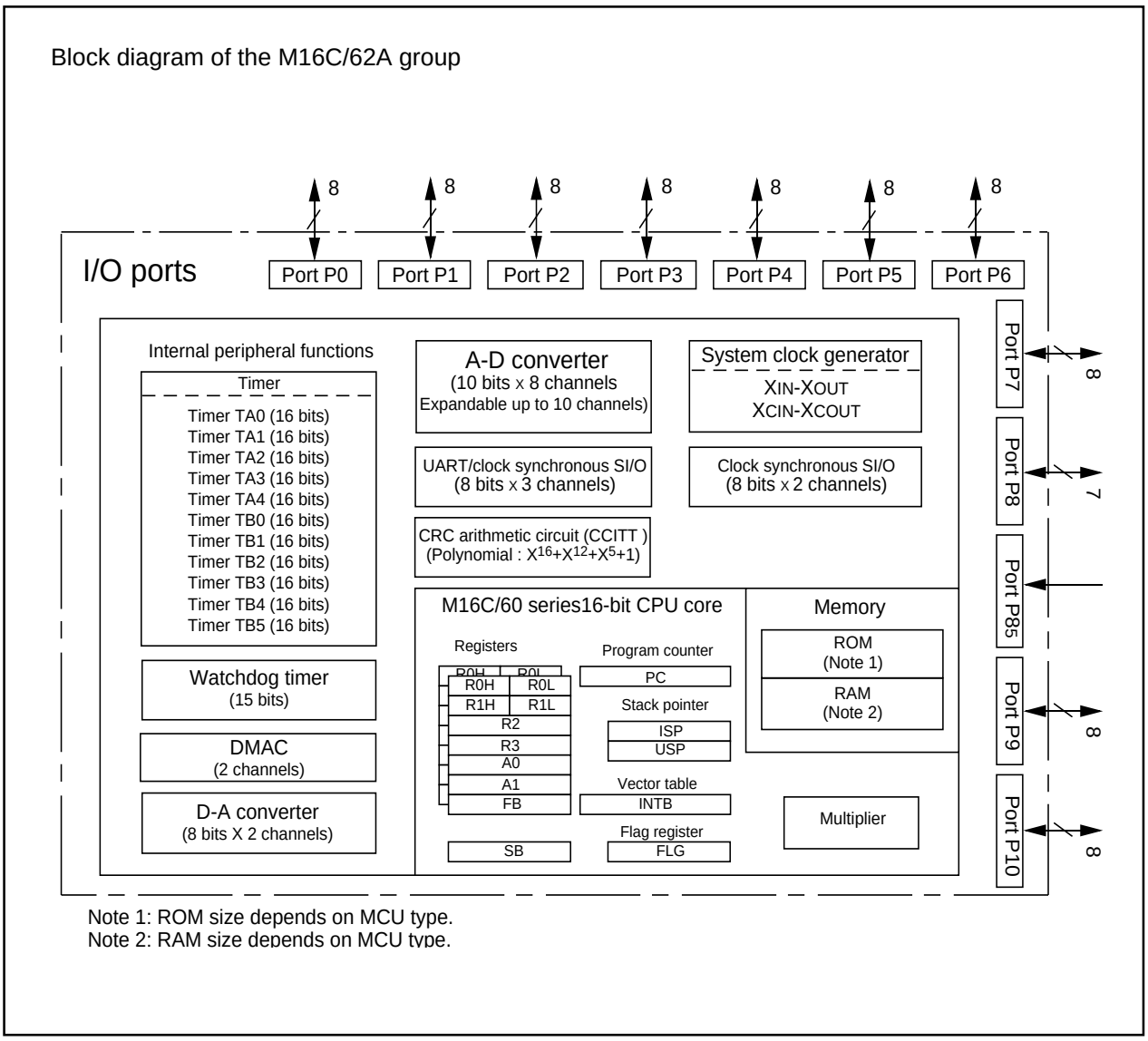


Figure 1.1.3. Block diagram of M16C/62A group

Performance Outline

Table 1.1.1 is a performance outline of M16C/62A group.

Table 1.1.1. Performance outline of M16C/62A group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		62.5ns(f(XIN)=16MHz, VCC=5V) 100ns (f(XIN)=10MHz, VCC=3V, with software one-wait) : Mask ROM, flash memory 5V version
Memory capacity	ROM	(See the figure 1.1.4. ROM Expansion)
	RAM	3K to 20K bytes
I/O port	P0 to P10 (except P85)	8 bits x 10, 7 bits x 1
Input port	P85	1 bit x 1
Multifunction timer	TA0, TA1, TA2, TA3, TA4	16 bits x 5
	TB0, TB1, TB2, TB3, TB4, TB5	16 bits x 6
Serial I/O	UART0, UART1, UART2	(UART or clock synchronous) x 3
	SI/O3, SI/O4	(Clock synchronous) x 2
A-D converter		10 bits x (8 + 2) channels
D-A converter		8 bits x 2
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		CRC-CCITT
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels
Clock generating circuit		2 built-in clock generation circuits (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage		4.2V to 5.5V (f(XIN)=16MHz, without software wait) : Mask ROM, flash memory 5V version 2.7V to 5.5V (f(XIN)=10MHz with software one-wait) : Mask ROM, flash memory 5V version
Power consumption		25.5mW (f(XIN) = 10MHz, VCC=3V with software one-wait)
I/O characteristics	I/O withstand voltage	5V
	Output current	5mA
Memory expansion		Available (to a maximum of 1M bytes)
Device configuration		CMOS high performance silicon gate
Package		100-pin plastic mold QFP

Mitsubishi plans to release the following products in the M16C/62A group:

(1) Support for mask ROM version, external ROM version, and flash memory version

(2) ROM capacity

(3) Package

100P6S-A : Plastic molded QFP (mask ROM, one-time PROM, and flash memory versions)

100P6Q-A : Plastic molded QFP(mask ROM, one-time PROM, and flash memory versions)

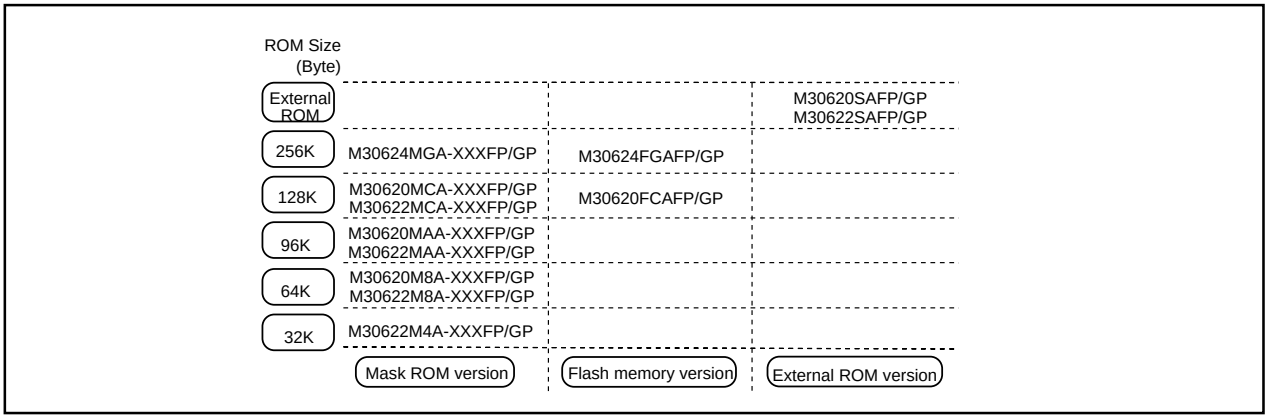


Figure 1.1.4. ROM expansion

The M16C/62A group products currently supported are listed in Table 1.1.2.

Table 1.1.2. M16C/62A group

December. 1999

Type No	ROM capacity	RAM capacity	Package type	Remarks
M30622M4A-XXXFP **	32K byte	3K byte	100P6S-A	Mask ROM version
M30622M4A-XXXGP **			100P6Q-A	
M30620M8A-XXXFP **	64K byte	10K byte	100P6S-A	
M30620M8A-XXXGP **			100P6Q-A	
M30622M8A-XXXFP **		4K byte	100P6S-A	
M30622M8A-XXXGP **			100P6Q-A	
M30620MAA-XXXFP **	96K byte	10K byte	100P6S-A	
M30620MAA-XXXGP **			100P6Q-A	
M30622MAA-XXXFP **		5K byte	100P6S-A	
M30622MAA-XXXGP **			100P6Q-A	
M30620MCA-XXXFP **	128K byte	10K byte	100P6S-A	
M30620MCA-XXXGP **			100P6Q-A	
M30622MCA-XXXFP **		5K byte	100P6S-A	
M30622MCA-XXXGP **			100P6Q-A	
M30624MGA-XXXFP **	256K byte	20K byte	100P6S-A	
M30624MGA-XXXGP **			100P6Q-A	
M30620FCAFP **	128K byte	10K byte	100P6S-A	Flash memory 5V version
M30620FCAGP **			100P6Q-A	
M30624FGAFP **	256K byte	20K byte	100P6S-A	
M30624FGAGP **			100P6Q-A	
M30620SAFP **	———	10K byte	100P6S-A	External ROM version
M30620SAGP **			100P6Q-A	
M30622SAFP **		3K byte	100P6S-A	
M30622SAGP **			100P6QA-A	

**: Under development

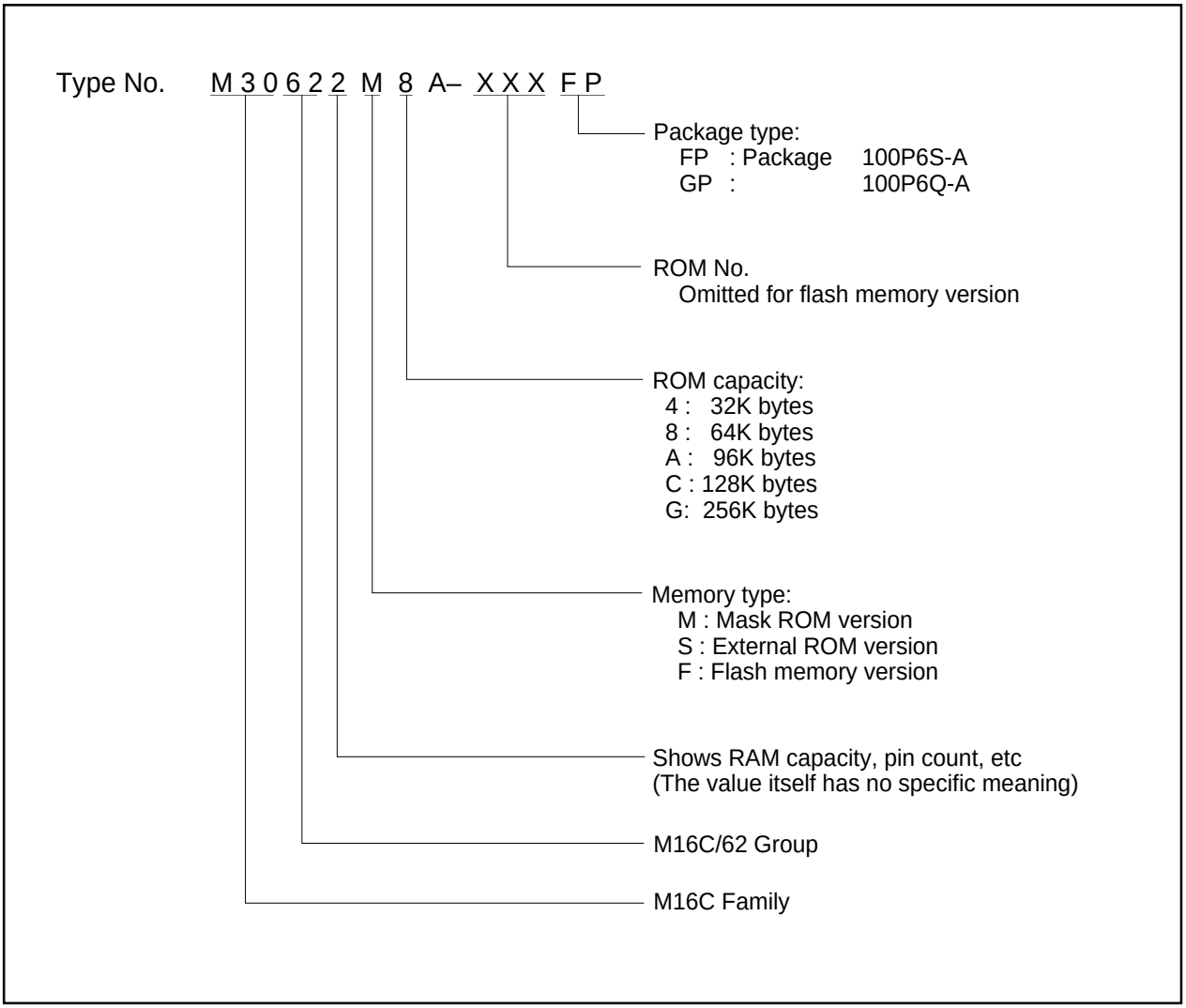


Figure 1.1.5. Type No., memory size, and package

Pin Description

Pin name	Signal name	I/O type	Function
V_{CC}, V_{SS}	Power supply input		Supply 2.7 to 5.5 V to the V_{CC} pin. Supply 0 V to the V_{SS} pin.
CNV$_{SS}$	CNV$_{SS}$	Input	This pin switches between processor modes. Connect this pin to the V_{SS} pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the V_{CC} pin when starting operation in microprocessor mode.
$\overline{\text{RESET}}$	Reset input	Input	A "L" on this input resets the microcomputer.
X_{IN} X_{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit.Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
BYTE	External data bus width select input	Input	This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the V_{SS} pin when not using external data bus.
AV$_{CC}$	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{CC}.
AV$_{SS}$	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{SS}.
V_{REF}	Reference voltage input	Input	This pin is a reference voltage input for the A-D converter.
$P0_0$ to $P0_7$	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input in single-chip mode, the port can be set to have or not have a pull-up resistor in units of four bits by software. In memory expansion and microprocessor modes, selection of the internal pull-resistor is not available.
D_0 to D_7		Input/output	When set as a separate bus, these pins input and output data (D_0–D_7).
$P1_0$ to $P1_7$	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as external interrupt pins as selected by software.
D_8 to D_{15}		Input/output	When set as a separate bus, these pins input and output data (D_8–D_{15}).
$P2_0$ to $P2_7$	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0.
A_0 to A_7		Output	These pins output 8 low-order address bits (A_0–A_7).
A_0/D_0 to A_7/D_7		Input/output	If the external bus is set as an 8-bit wide multiplexed bus, these pins input and output data (D_0–D_7) and output 8 low-order address bits (A_0–A_7) separated in time by multiplexing.
A_0, A_1/D_0 to A_7/D_6		Output Input/output	If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D_0–D_6) and output address (A_1–A_7) separated in time by multiplexing. They also output address (A_0).
$P3_0$ to $P3_7$	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0.
A_8 to A_{15}		Output	These pins output 8 middle-order address bits (A_8–A_{15}).
A_8/D_7, A_9 to A_{15}		Input/output Output	If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D_7) and output address (A_8) separated in time by multiplexing. They also output address (A_9–A_{15}).
$P4_0$ to $P4_7$	I/O port P4	Input/output	This is an 8-bit I/O port equivalent to P0.
$\overline{CS_0}$ to $\overline{CS_3}$, A_{16} to A_{19}		Output Output	These pins output $\overline{CS_0}$–$\overline{CS_3}$ signals and A_{16}–A_{19}. $\overline{CS_0}$–$\overline{CS_3}$ are chip select signals used to specify an access space. A_{16}–A_{19} are 4 high-order address bits.

Pin Description

Pin name	Signal name	I/O type	Function
P5$_0$ to P5$_7$	I/O port P5	Input/output	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P5$_7$ in this port outputs a divide-by-8 or divide-by-32 clock of X_{IN} or a clock of the same frequency as X_{CIN} as selected by software.
$\overline{WRL}$ / $\overline{WR}$, WRH / $\overline{BHE}$, $\overline{RD}$, BCLK, $\overline{HLDA}$, $\overline{HOLD}$, ALE, $\overline{RDY}$		Output Output Output Output Output Input Output Input	Output $\overline{WRL}$, $\overline{WRH}$ ($\overline{WR}$ and $\overline{BHE}$), $\overline{RD}$, BCLK, $\overline{HLDA}$, and ALE signals. $\overline{WRL}$ and $\overline{WRH}$, and $\overline{BHE}$ and $\overline{WR}$ can be switched using software control. ■ $\overline{WRL}$, $\overline{WRH}$, and $\overline{RD}$ selected With a 16-bit external data bus, data is written to even addresses when the $\overline{WRL}$ signal is "L" and to the odd addresses when the $\overline{WRH}$ signal is "L". Data is read when $\overline{RD}$ is "L". ■ $\overline{WR}$, $\overline{BHE}$, and $\overline{RD}$ selected Data is written when $\overline{WR}$ is "L". Data is read when $\overline{RD}$ is "L". Odd addresses are accessed when $\overline{BHE}$ is "L". Use this mode when using an 8-bit external data bus. While the input level at the $\overline{HOLD}$ pin is "L", the microcomputer is placed in the hold state. While in the hold state, $\overline{HLDA}$ outputs a "L" level. ALE is used to latch the address. While the input level of the $\overline{RDY}$ pin is "L", the microcomputer is in the ready state.
P6$_0$ to P6$_7$	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. When used for input in single-chip, memory expansion, and microprocessor modes, the port can be set to have or not have a pull-up resistor in units of four bits by software. Pins in this port also function as UART0 and UART1 I/O pins as selected by software.
P7$_0$ to P7$_7$	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P6 (P7$_0$ and P7$_1$ are N channel open-drain output). Pins in this port also function as timer A$_0$–A$_3$, timer B5 or UART2 I/O pins as selected by software.
P8$_0$ to P8$_4$, P8$_6$, P8$_7$, P8$_5$	I/O port P8 I/O port P8$_5$	Input/output Input/output Input/output Input	P8$_0$ to P8$_4$, P8$_6$, and P8$_7$ are I/O ports with the same functions as P6. Using software, they can be made to function as the I/O pins for timer A4 and the input pins for external interrupts. P8$_6$ and P8$_7$ can be set using software to function as the I/O pins for a sub clock generation circuit. In this case, connect a quartz oscillator between P8$_6$ (X_{COUT} pin) and P8$_7$ (X_{CIN} pin). P8$_5$ is an input-only port that also functions for $\overline{NMI}$. The $\overline{NMI}$ interrupt is generated when the input at this pin changes from "H" to "L". The $\overline{NMI}$ function cannot be cancelled using software. The pull-up cannot be set for this pin.
P9$_0$ to P9$_7$	I/O port P9	Input/output	This is an 8-bit I/O port equivalent to P6. Pins in this port also function as SI/O3, 4 I/O pins, Timer B0–B4 input pins, D-A converter output pins, A-D converter extended input pins, or A-D trigger input pins as selected by software.
P10$_0$ to P10$_7$	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P6. Pins in this port also function as A-D converter input pins. Furthermore, P10$_4$–P10$_7$ also function as input pins for the key input interrupt function.

Operation of Functional Blocks

The M16C/62A group accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, serial I/O, D-A converter, DMAC, CRC calculation circuit, A-D converter, and I/O ports.

The following explains each unit.

Memory

Figure 1.3.1 is a memory map of the M16C/62A group. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$. From $FFFFF_{16}$ down is ROM. For example, in the M30622MCA-XXXFP, there is 128K bytes of internal ROM from $E0000_{16}$ to $FFFFF_{16}$. The vector table for fixed interrupts such as the reset and $\overline{NMI}$ are mapped to $FFFDC_{16}$ to $FFFFF_{16}$. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

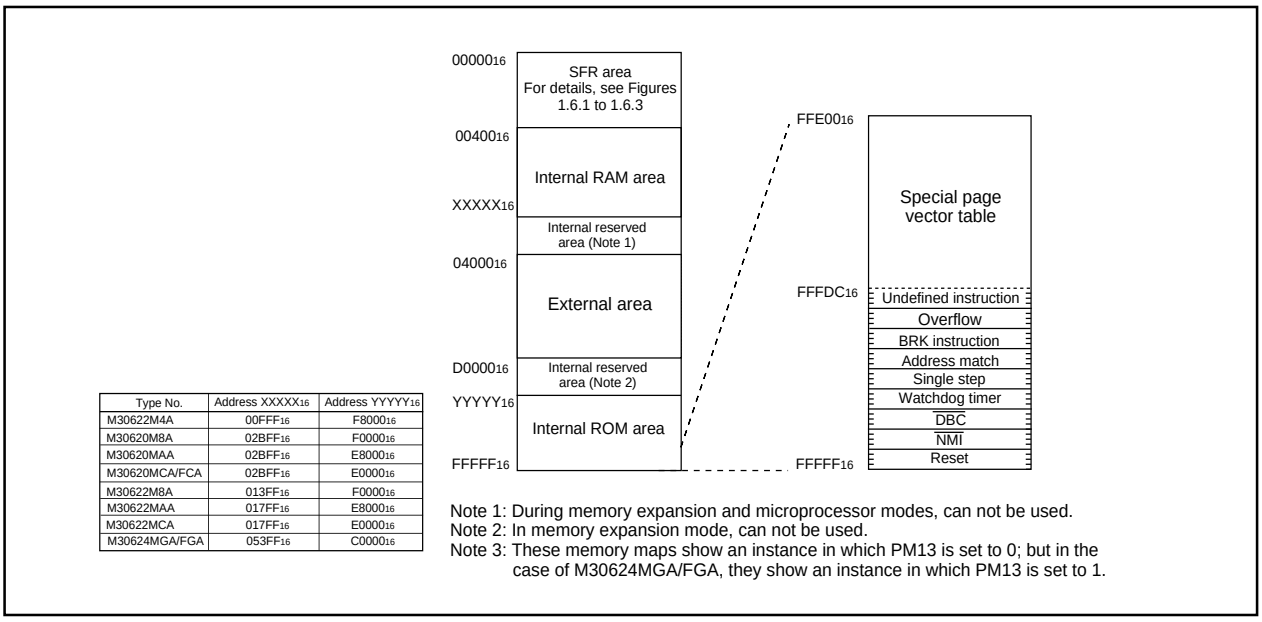
From 00400_{16} up is RAM. For example, in the M30622MCA-XXXFP, 5K bytes of internal RAM is mapped to the space from 00400_{16} to $017FF_{16}$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000_{16} to $003FF_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Figures 1.6.1 to 1.6.3 are location of peripheral unit control registers. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to $FFE00_{16}$ to $FFFDB_{16}$. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

In memory expansion mode and microprocessor mode, a part of the spaces are reserved and cannot be used. For example, in the M30622MCA-XXXFP, the following spaces cannot be used.

- The space between 01800_{16} and $03FFF_{16}$ (Memory expansion and microprocessor modes)
- The space between $D0000_{16}$ and $D7FFF_{16}$ (Memory expansion mode)



Type No.	Address XXXXX$_{16}$	Address YYYYY$_{16}$
M30622M4A	00FFF$_{16}$	F8000$_{16}$
M30620M8A	02BFF$_{16}$	F0000$_{16}$
M30620MAA	02BFF$_{16}$	E8000$_{16}$
M30620MCA/FCA	02BFF$_{16}$	E0000$_{16}$
M30622M8A	013FF$_{16}$	F0000$_{16}$
M30622MAA	017FF$_{16}$	E8000$_{16}$
M30622MCA	017FF$_{16}$	E0000$_{16}$
M30624MGA/FGA	053FF$_{16}$	C0000$_{16}$

Note 1: During memory expansion and microprocessor modes, can not be used.
Note 2: In memory expansion mode, can not be used.
Note 3: These memory maps show an instance in which PM13 is set to 0; but in the case of M30624MGA/FGA, they show an instance in which PM13 is set to 1.

Figure 1.3.1. Memory map

Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.4.1. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

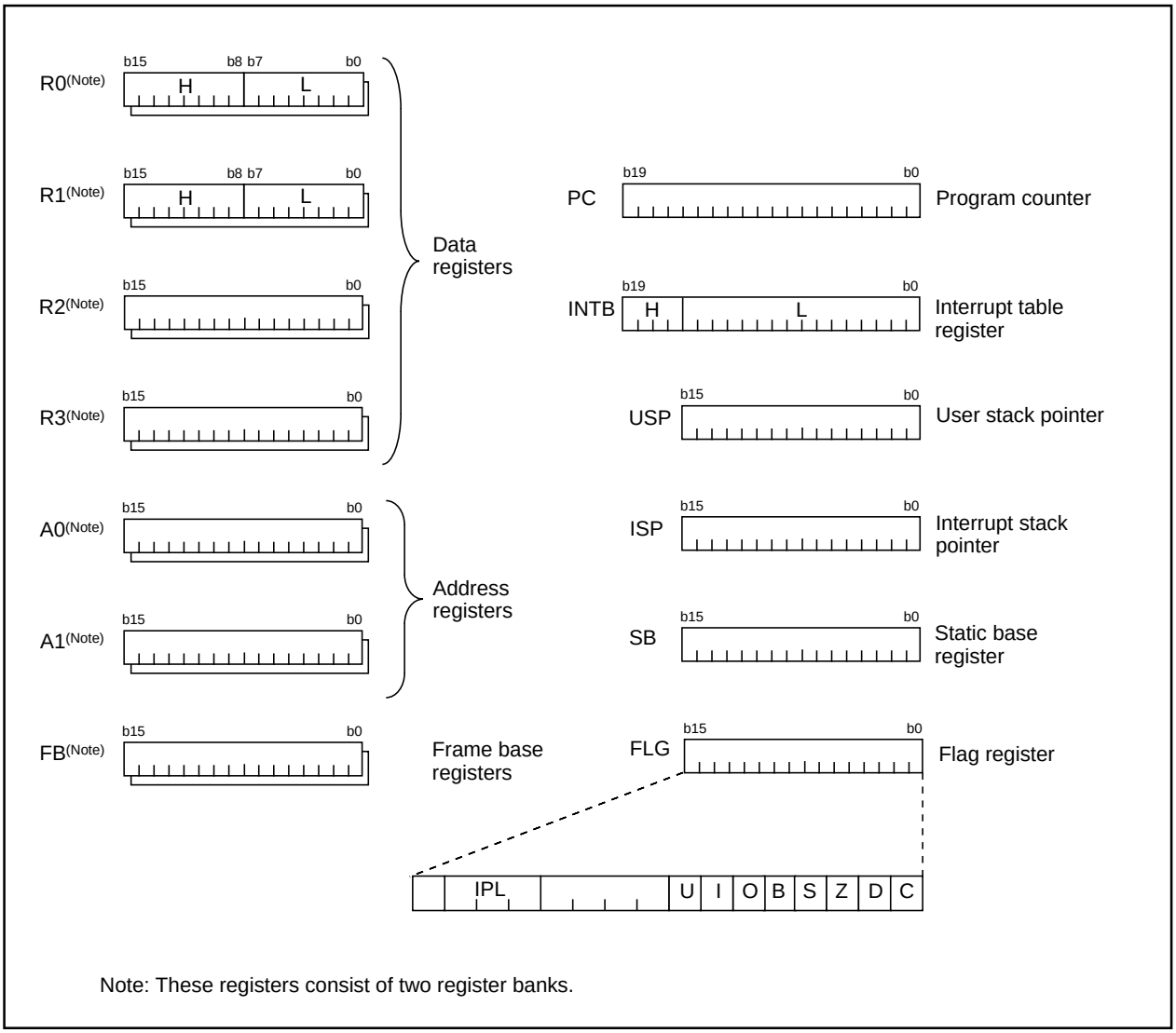


Figure 1.4.1. Central processing unit register

(1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H/R1H), and low-order bits as (R0L/R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0/R3R1).

(2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

(4) Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

(5) Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

(6) Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag). This flag is located at the position of bit 7 in the flag register (FLG).

(7) Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

(8) Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.4.2 shows the flag register (FLG). The following explains the function of each flag:

- **Bit 0: Carry flag (C flag)**
  This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.
- **Bit 1: Debug flag (D flag)**
  This flag enables a single-step interrupt.
  When this flag is “1”, a single-step interrupt is generated after instruction execution. This flag is cleared to “0” when the interrupt is acknowledged.
- **Bit 2: Zero flag (Z flag)**
  This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, cleared to “0”.
- **Bit 3: Sign flag (S flag)**
  This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, cleared to “0”.
- **Bit 4: Register bank select flag (B flag)**
  This flag chooses a register bank. Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.
- **Bit 5: Overflow flag (O flag)**
  This flag is set to “1” when an arithmetic operation resulted in overflow; otherwise, cleared to “0”.
- **Bit 6: Interrupt enable flag (I flag)**
  This flag enables a maskable interrupt.
  An interrupt is disabled when this flag is “0”, and is enabled when this flag is “1”. This flag is cleared to “0” when the interrupt is acknowledged.

- **Bit 7: Stack pointer select flag (U flag)**
  Interrupt stack pointer (ISP) is selected when this flag is “0” ; user stack pointer (USP) is selected when this flag is “1”.
  This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.
- **Bits 8 to 11: Reserved area**
- **Bits 12 to 14: Processor interrupt priority level (IPL)**
  Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
  If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.
- **Bit 15: Reserved area**

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

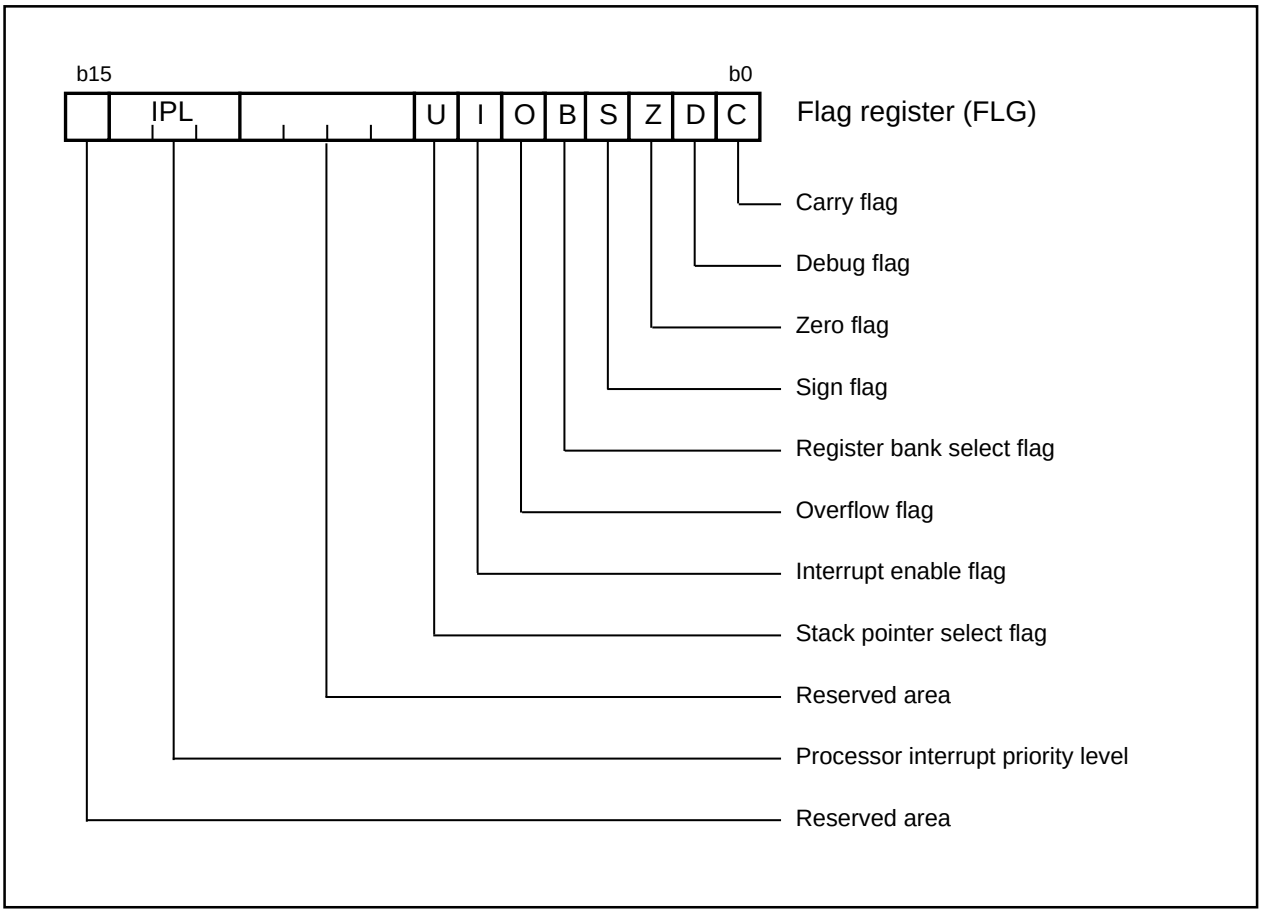


Figure 1.4.2. Flag register (FLG)

Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See “Software Reset” for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level “L” (0.2VCC max.) for at least 20 cycles. When the reset pin level is then returned to the “H” level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.5.1 shows the example reset circuit. Figure 1.5.2 shows the reset sequence.

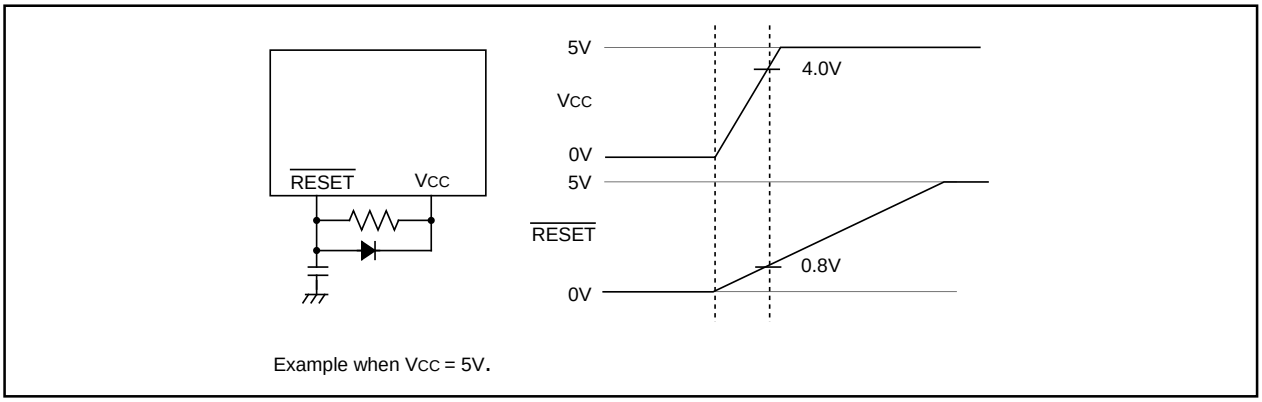


Figure 1.5.1. Example reset circuit

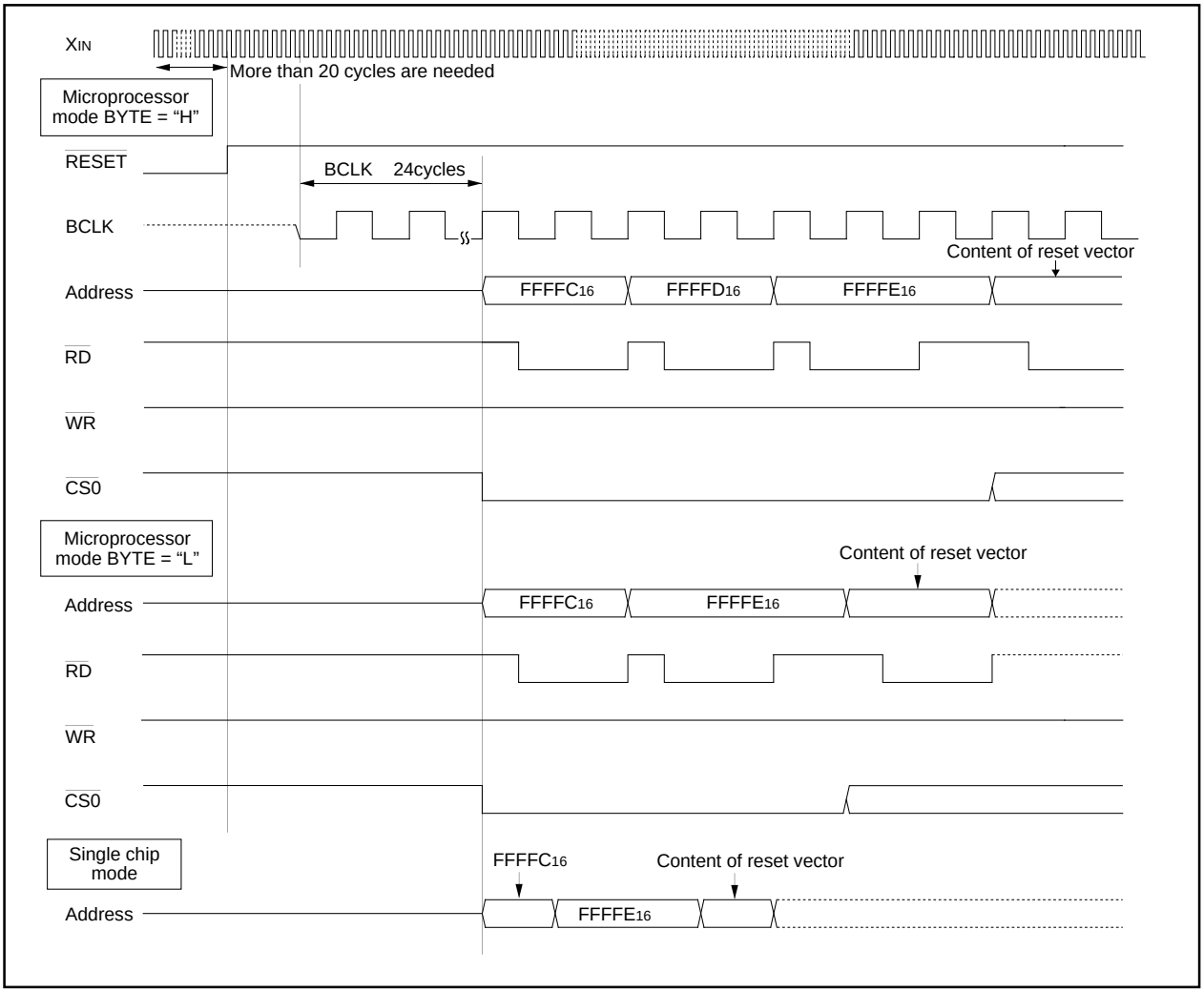
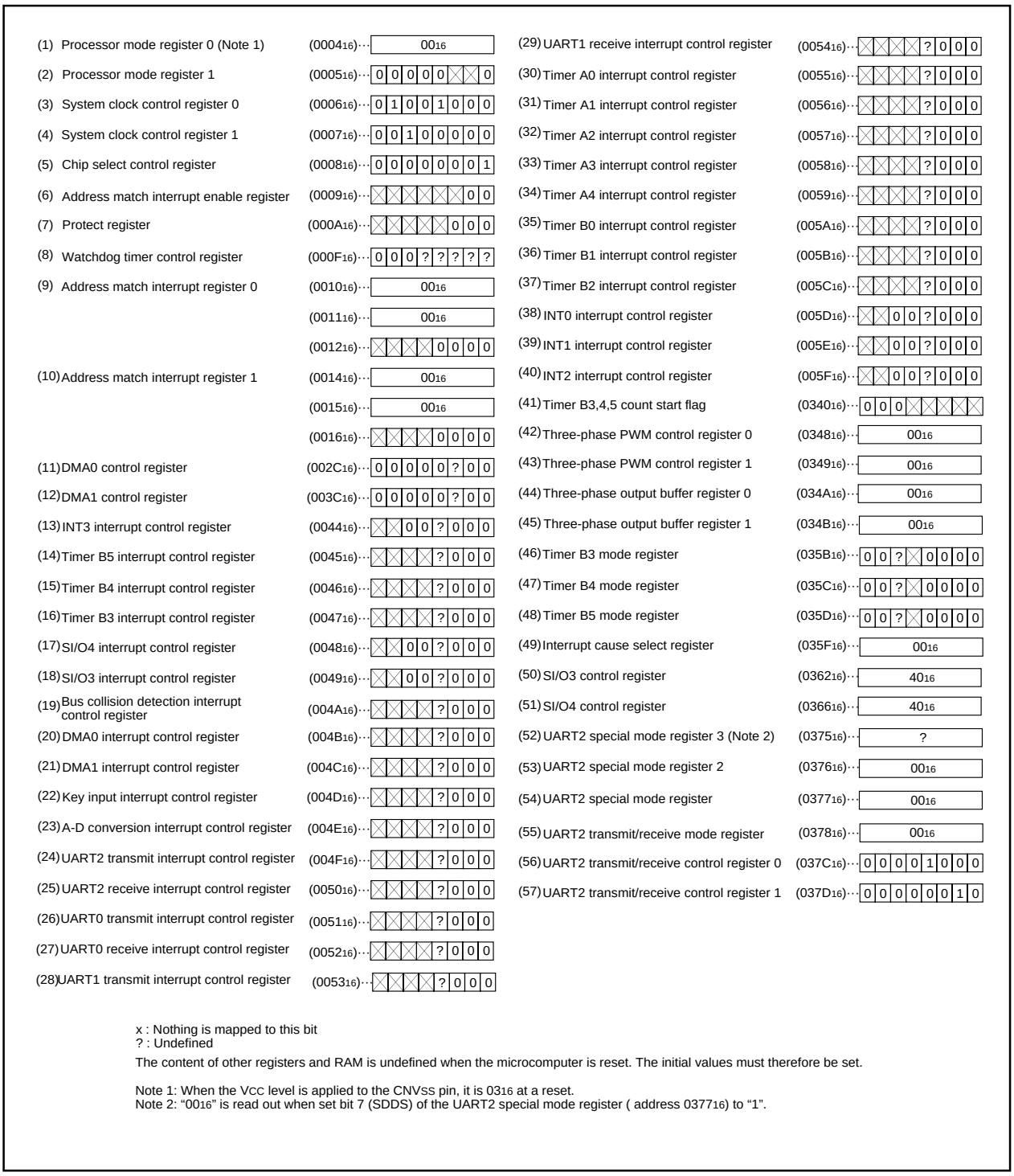


Figure 1.5.2. Reset sequence

Table 1.5.1 shows the statuses of the other pins while the $\overline{\text{RESET}}$ pin level is “L”. Figures 1.5.3 and 1.5.4 show the internal status of the microcomputer immediately after the reset is cancelled.

Table 1.5.1. Pin status when $\overline{\text{RESET}}$ pin level is “L”

Pin name	Status		
	CNVSS = VSS	CNVSS = VCC	
		BYTE = VSS	BYTE = VCC
P0	Input port (floating)	Data input (floating)	Data input (floating)
P1	Input port (floating)	Data input (floating)	Input port (floating)
P2, P3, P40 to P43	Input port (floating)	Address output (undefined)	Address output (undefined)
P44	Input port (floating)	$\overline{\text{CS0}}$ output (“H” level is output)	$\overline{\text{CS0}}$ output (“H” level is output)
P45 to P47	Input port (floating)	Input port (floating) (pull-up resistor is on)	Input port (floating) (pull-up resistor is on)
P50	Input port (floating)	$\overline{\text{WR}}$ output (“H” level is output)	$\overline{\text{WR}}$ output (“H” level is output)
P51	Input port (floating)	$\overline{\text{BHE}}$ output (undefined)	$\overline{\text{BHE}}$ output (undefined)
P52	Input port (floating)	$\overline{\text{RD}}$ output (“H” level is output)	$\overline{\text{RD}}$ output (“H” level is output)
P53	Input port (floating)	BCLK output	BCLK output
P54	Input port (floating)	$\overline{\text{HLDA}}$ output (The output value depends on the input to the $\overline{\text{HOLD}}$ pin)	$\overline{\text{HLDA}}$ output (The output value depends on the input to the $\overline{\text{HOLD}}$ pin)
P55	Input port (floating)	$\overline{\text{HOLD}}$ input (floating)	$\overline{\text{HOLD}}$ input (floating)
P56	Input port (floating)	ALE output (“L” level is output)	ALE output (“L” level is output)
P57	Input port (floating)	$\overline{\text{RDY}}$ input (floating)	$\overline{\text{RDY}}$ input (floating)
P6, P7, P80 to P84, P86, P87, P9, P10	Input port (floating)	Input port (floating)	Input port (floating)



x : Nothing is mapped to this bit
? : Undefined

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

Note 1: When the V_{CC} level is applied to the CNV_{SS} pin, it is 03_{16} at a reset.
Note 2: "00_{16}" is read out when set bit 7 (SDDS) of the UART2 special mode register (address 0377_{16}) to "1".

Figure 1.5.3. Device's internal status after a reset is cleared

(58) Count start flag	(0380_{16})···	00_{16}	(84) A-D control register 1	($03D7_{16}$)···	00_{16}
(59) Clock prescaler reset flag	(0381_{16})···	0 x x x x x x x	(85) D-A control register	($03DC_{16}$)···	00_{16}
(60) One-shot start flag	(0382_{16})···	0 0 x 0 0 0 0 0	(86) Port P0 direction register	($03E2_{16}$)···	00_{16}
(61) Trigger select flag	(0383_{16})···	00_{16}	(87) Port P1 direction register	($03E3_{16}$)···	00_{16}
(62) Up-down flag	(0384_{16})···	00_{16}	(88) Port P2 direction register	($03E6_{16}$)···	00_{16}
(63) Timer A0 mode register	(0396_{16})···	00_{16}	(89) Port P3 direction register	($03E7_{16}$)···	00_{16}
(64) Timer A1 mode register	(0397_{16})···	00_{16}	(90) Port P4 direction register	($03EA_{16}$)···	00_{16}
(65) Timer A2 mode register	(0398_{16})···	00_{16}	(91) Port P5 direction register	($03EB_{16}$)···	00_{16}
(66) Timer A3 mode register	(0399_{16})···	00_{16}	(92) Port P6 direction register	($03EE_{16}$)···	00_{16}
(67) Timer A4 mode register	($039A_{16}$)···	00_{16}	(93) Port P7 direction register	($03EF_{16}$)···	00_{16}
(68) Timer B0 mode register	($039B_{16}$)···	0 0 ? x 0 0 0 0	(94) Port P8 direction register	($03F2_{16}$)···	0 0 x 0 0 0 0 0
(69) Timer B1 mode register	($039C_{16}$)···	0 0 ? x 0 0 0 0	(95) Port P9 direction register	($03F3_{16}$)···	00_{16}
(70) Timer B2 mode register	($039D_{16}$)···	0 0 ? x 0 0 0 0	(96) Port P10 direction register	($03F6_{16}$)···	00_{16}
(71) UART0 transmit/receive mode register	($03A0_{16}$)···	00_{16}	(97) Pull-up control register 0	($03FC_{16}$)···	00_{16}
(72) UART0 transmit/receive control register 0	($03A4_{16}$)···	0 0 0 0 1 0 0 0	(98) Pull-up control register 1(Note1)	($03FD_{16}$)···	00_{16}
(73) UART0 transmit/receive control register 1	($03A5_{16}$)···	0 0 0 0 0 0 1 0	(99) Pull-up control register 2	($03FE_{16}$)···	00_{16}
(74) UART1 transmit/receive mode register	($03A8_{16}$)···	00_{16}	(100) Port control register	($03FF_{16}$)···	00_{16}
(75) UART1 transmit/receive control register 0	($03AC_{16}$)···	0 0 0 0 1 0 0 0	(101) Data registers (R0/R1/R2/R3)		0000_{16}
(76) UART1 transmit/receive control register 1	($03AD_{16}$)···	0 0 0 0 0 0 1 0	(102) Address registers (A0/A1)		0000_{16}
(77) UART transmit/receive control register 2	($03B0_{16}$)···	x 0 0 0 0 0 0 0	(103) Frame base register (FB)		0000_{16}
(78) Flash memory control register 1 (Note2)	($03B6_{16}$)···	? ? ? ? 0 ? ? ?	(104) Interrupt table register (INTB)		00000_{16}
(79) Flash memory control register 0 (Note2)	($03B7_{16}$)···	x x 0 0 0 0 0 1	(105) User stack pointer (USP)		0000_{16}
(80) DMA0 cause select register	($03B8_{16}$)···	00_{16}	(106) Interrupt stack pointer (ISP)		0000_{16}
(81) DMA1 cause select register	($03BA_{16}$)···	00_{16}	(107) Static base register (SB)		0000_{16}
(82) A-D control register 2	($03D4_{16}$)···	0 0 0 0 x x x 0	(108) Flag register (FLG)		0000_{16}
(83) A-D control register 0	($03D6_{16}$)···	0 0 0 0 0 ? ? ?			

x : Nothing is mapped to this bit
? : Undefined

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

Note1: When the V_{CC} level is applied to the CNV_{SS} pin, it is 02_{16} at a reset.
Note2: This register is only exist in flash memory version.

Figure 1.5.4. Device's internal status after a reset is cleared

0000₁₆	
0001₁₆	
0002₁₆	
0003₁₆	
0004₁₆	Processor mode register 0 (PM0)
0005₁₆	Processor mode register 1(PM1)
0006₁₆	System clock control register 0 (CM0)
0007₁₆	System clock control register 1 (CM1)
0008₁₆	Chip select control register (CSR)
0009₁₆	Address match interrupt enable register (AIER)
000A₁₆	Protect register (PRCR)
000B₁₆	
000C₁₆	
000D₁₆	
000E₁₆	Watchdog timer start register (WDTS)
000F₁₆	Watchdog timer control register (WDC)
0010₁₆	Address match interrupt register 0 (RMAD0)
0011₁₆	
0012₁₆	
0013₁₆	
0014₁₆	Address match interrupt register 1 (RMAD1)
0015₁₆	
0016₁₆	
0017₁₆	
0018₁₆	
0019₁₆	
001A₁₆	
001B₁₆	
001C₁₆	
001D₁₆	
001E₁₆	
001F₁₆	
0020₁₆	DMA0 source pointer (SAR0)
0021₁₆	
0022₁₆	
0023₁₆	
0024₁₆	DMA0 destination pointer (DAR0)
0025₁₆	
0026₁₆	
0027₁₆	
0028₁₆	DMA0 transfer counter (TCR0)
0029₁₆	
002A₁₆	
002B₁₆	
002C₁₆	DMA0 control register (DM0CON)
002D₁₆	
002E₁₆	
002F₁₆	
0030₁₆	DMA1 source pointer (SAR1)
0031₁₆	
0032₁₆	
0033₁₆	
0034₁₆	DMA1 destination pointer (DAR1)
0035₁₆	
0036₁₆	
0037₁₆	
0038₁₆	DMA1 transfer counter (TCR1)
0039₁₆	
003A₁₆	
003B₁₆	
003C₁₆	DMA1 control register (DM1CON)
003D₁₆	
003E₁₆	
003F₁₆	

0040₁₆	
0041₁₆	
0042₁₆	
0043₁₆	
0044₁₆	INT3 interrupt control register (INT3IC)
0045₁₆	Timer B5 interrupt control register (TB5IC)
0046₁₆	Timer B4 interrupt control register (TB4IC)
0047₁₆	Timer B3 interrupt control register (TB3IC)
0048₁₆	SI/O4 interrupt control register (S4IC) INT5 interrupt control register (INT5IC)
0049₁₆	SI/O3 interrupt control register (S3IC) INT4 interrupt control register (INT4IC)
004A₁₆	Bus collision detection interrupt control register (BCNIC)
004B₁₆	DMA0 interrupt control register (DM0IC)
004C₁₆	DMA1 interrupt control register (DM1IC)
004D₁₆	Key input interrupt control register (KUPIC)
004E₁₆	A-D conversion interrupt control register (ADIC)
004F₁₆	UART2 transmit interrupt control register (S2TIC)
0050₁₆	UART2 receive interrupt control register (S2RIC)
0051₁₆	UART0 transmit interrupt control register (S0TIC)
0052₁₆	UART0 receive interrupt control register (S0RIC)
0053₁₆	UART1 transmit interrupt control register (S1TIC)
0054₁₆	UART1 receive interrupt control register (S1RIC)
0055₁₆	Timer A0 interrupt control register (TA0IC)
0056₁₆	Timer A1 interrupt control register (TA1IC)
0057₁₆	Timer A2 interrupt control register (TA2IC)
0058₁₆	Timer A3 interrupt control register (TA3IC)
0059₁₆	Timer A4 interrupt control register (TA4IC)
005A₁₆	Timer B0 interrupt control register (TB0IC)
005B₁₆	Timer B1 interrupt control register (TB1IC)
005C₁₆	Timer B2 interrupt control register (TB2IC)
005D₁₆	INT0 interrupt control register (INT0IC)
005E₁₆	INT1 interrupt control register (INT1IC)
005F₁₆	INT2 interrupt control register (INT2IC)
0060₁₆	
0061₁₆	
0062₁₆	
0063₁₆	
0064₁₆	
0065₁₆	
≈	≈
032A₁₆	
032B₁₆	
032C₁₆	
032D₁₆	
032E₁₆	
032F₁₆	
0330₁₆	
0331₁₆	
0332₁₆	
0333₁₆	
0334₁₆	
0335₁₆	
0336₁₆	
0337₁₆	
0338₁₆	
0339₁₆	
033A₁₆	
033B₁₆	
033C₁₆	
033D₁₆	
033E₁₆	
033F₁₆	

Note 1: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.6.1. Location of peripheral unit control registers (1)

0340₁₆	Timer B3, 4, 5 count start flag (TBSR)
0341₁₆	
0342₁₆ 0343₁₆	Timer A1-1 register (TA11)
0344₁₆ 0345₁₆	Timer A2-1 register (TA21)
0346₁₆ 0347₁₆	Timer A4-1 register (TA41)
0348₁₆	Three-phase PWM control register 0(INVC0)
0349₁₆	Three-phase PWM control register 1(INVC1)
034A₁₆	Three-phase output buffer register 0(IDB0)
034B₁₆	Three-phase output buffer register 1(IDB1)
034C₁₆	Dead time timer(DTT)
034D₁₆	Timer B2 interrupt occurrence frequency set counter(ICTB2)
034E₁₆	
034F₁₆	
0350₁₆ 0351₁₆	Timer B3 register (TB3)
0352₁₆ 0353₁₆	Timer B4 register (TB4)
0354₁₆ 0355₁₆	Timer B5 register (TB5)
0356₁₆	
0357₁₆	
0358₁₆	
0359₁₆	
035A₁₆	
035B₁₆	Timer B3 mode register (TB3MR)
035C₁₆	Timer B4 mode register (TB4MR)
035D₁₆	Timer B5 mode register (TB5MR)
035E₁₆	
035F₁₆	Interrupt cause select register (IFSR)
0360₁₆	SI/O3 transmit/receive register (S3TRR)
0361₁₆	
0362₁₆	SI/O3 control register (S3C)
0363₁₆	SI/O3 bit rate generator (S3BRG)
0364₁₆	SI/O4 transmit/receive register (S4TRR)
0365₁₆	
0366₁₆	SI/O4 control register (S4C)
0367₁₆	SI/O4 bit rate generator (S4BRG)
0368₁₆	
0369₁₆	
036A₁₆	
036B₁₆	
036C₁₆	
036D₁₆	
036E₁₆	
036F₁₆	
0370₁₆	
0371₁₆	
0372₁₆	
0373₁₆	
0374₁₆	
0375₁₆	UART2 special mode register 3(U2SMR3)
0376₁₆	UART2 special mode register 2(U2SMR2)
0377₁₆	UART2 special mode register (U2SMR)
0378₁₆	UART2 transmit/receive mode register (U2MR)
0379₁₆	UART2 bit rate generator (U2BRG)
037A₁₆ 037B₁₆	UART2 transmit buffer register (U2TB)
037C₁₆	UART2 transmit/receive control register 0 (U2C0)
037D₁₆	UART2 transmit/receive control register 1 (U2C1)
037E₁₆ 037F₁₆	UART2 receive buffer register (U2RB)

0380₁₆	Count start flag (TABSR)
0381₁₆	Clock prescaler reset flag (CPSRF)
0382₁₆	One-shot start flag (ONSF)
0383₁₆	Trigger select register (TRGSR)
0384₁₆	Up-down flag (UDF)
0385₁₆	
0386₁₆ 0387₁₆	Timer A0 (TA0)
0388₁₆ 0389₁₆	Timer A1 (TA1)
038A₁₆ 038B₁₆	Timer A2 (TA2)
038C₁₆ 038D₁₆	Timer A3 (TA3)
038E₁₆ 038F₁₆	Timer A4 (TA4)
0390₁₆ 0391₁₆	Timer B0 (TB0)
0392₁₆ 0393₁₆	Timer B1 (TB1)
0394₁₆ 0395₁₆	Timer B2 (TB2)
0396₁₆	Timer A0 mode register (TA0MR)
0397₁₆	Timer A1 mode register (TA1MR)
0398₁₆	Timer A2 mode register (TA2MR)
0399₁₆	Timer A3 mode register (TA3MR)
039A₁₆	Timer A4 mode register (TA4MR)
039B₁₆	Timer B0 mode register (TB0MR)
039C₁₆	Timer B1 mode register (TB1MR)
039D₁₆	Timer B2 mode register (TB2MR)
039E₁₆	
039F₁₆	
03A0₁₆	UART0 transmit/receive mode register (U0MR)
03A1₁₆	UART0 bit rate generator (U0BRG)
03A2₁₆ 03A3₁₆	UART0 transmit buffer register (U0TB)
03A4₁₆	UART0 transmit/receive control register 0 (U0C0)
03A5₁₆	UART0 transmit/receive control register 1 (U0C1)
03A6₁₆ 03A7₁₆	UART0 receive buffer register (U0RB)
03A8₁₆	UART1 transmit/receive mode register (U1MR)
03A9₁₆	UART1 bit rate generator (U1BRG)
03AA₁₆ 03AB₁₆	UART1 transmit buffer register (U1TB)
03AC₁₆	UART1 transmit/receive control register 0 (U1C0)
03AD₁₆	UART1 transmit/receive control register 1 (U1C1)
03AE₁₆ 03AF₁₆	UART1 receive buffer register (U1RB)
03B0₁₆	UART transmit/receive control register 2 (UCON)
03B1₁₆	
03B2₁₆	
03B3₁₆	
03B4₁₆	
03B5₁₆	
03B6₁₆	Flash memory control register 1 (FMR1) (Note1)
03B7₁₆	Flash memory control register 0 (FMR0) (Note1)
03B8₁₆	DMA0 request cause select register (DM0SL)
03B9₁₆	
03BA₁₆	DMA1 request cause select register (DM1SL)
03BB₁₆	
03BC₁₆ 03BD₁₆	CRC data register (CRCD)
03BE₁₆	CRC input register (CRCIN)
03BF₁₆	

Note 1: This register is only exist in flash memory version.
Note 2: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.6.2. Location of peripheral unit control registers (2)

03C0₁₆ 03C1₁₆	A-D register 0 (AD0)
03C2₁₆ 03C3₁₆	A-D register 1 (AD1)
03C4₁₆ 03C5₁₆	A-D register 2 (AD2)
03C6₁₆ 03C7₁₆	A-D register 3 (AD3)
03C8₁₆ 03C9₁₆	A-D register 4 (AD4)
03CA₁₆ 03CB₁₆	A-D register 5 (AD5)
03CC₁₆ 03CD₁₆	A-D register 6 (AD6)
03CE₁₆ 03CF₁₆	A-D register 7 (AD7)
03D0₁₆	
03D1₁₆	
03D2₁₆	
03D3₁₆	
03D4₁₆	A-D control register 2 (ADCON2)
03D5₁₆	
03D6₁₆	A-D control register 0 (ADCON0)
03D7₁₆	A-D control register 1 (ADCON1)
03D8₁₆	D-A register 0 (DA0)
03D9₁₆	
03DA₁₆	D-A register 1 (DA1)
03DB₁₆	
03DC₁₆	D-A control register (DACON)
03DD₁₆	
03DE₁₆	
03DF₁₆	
03E0₁₆	Port P0 (P0)
03E1₁₆	Port P1 (P1)
03E2₁₆	Port P0 direction register (PD0)
03E3₁₆	Port P1 direction register (PD1)
03E4₁₆	Port P2 (P2)
03E5₁₆	Port P3 (P3)
03E6₁₆	Port P2 direction register (PD2)
03E7₁₆	Port P3 direction register (PD3)
03E8₁₆	Port P4 (P4)
03E9₁₆	Port P5 (P5)
03EA₁₆	Port P4 direction register (PD4)
03EB₁₆	Port P5 direction register (PD5)
03EC₁₆	Port P6 (P6)
03ED₁₆	Port P7 (P7)
03EE₁₆	Port P6 direction register (PD6)
03EF₁₆	Port P7 direction register (PD7)
03F0₁₆	Port P8 (P8)
03F1₁₆	Port P9 (P9)
03F2₁₆	Port P8 direction register (PD8)
03F3₁₆	Port P9 direction register (PD9)
03F4₁₆	Port P10 (P10)
03F5₁₆	
03F6₁₆	Port P10 direction register (PD10)
03F7₁₆	
03F8₁₆	
03F9₁₆	
03FA₁₆	
03FB₁₆	
03FC₁₆	Pull-up control register 0 (PUR0)
03FD₁₆	Pull-up control register 1 (PUR1)
03FE₁₆	Pull-up control register 2 (PUR2)
03FF₁₆	Port control register (PCR)

Note : Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.6.3. Location of peripheral unit control registers (3)