5V to 12V Supply Voltage, 8-PIN, Synchronous Buck PWM Controller

Features

- Operating with Single 5~12V Supply Voltage or two Supply Voltages
- Drive Dual Low Cost N-Channel MOSFETs
  - Adaptive Shoot-Through Protection
- Built-in Feedback Compensation
  - Voltage-Mode PWM Control
  - 0~100% Duty Ratio
  - Fast Transient Response
- ±2% 0.8V Reference
  - Over Line, Load Regulation and Operating Temp.
- Programmable Over-Current Protection
  - Using $R_{DS(ON)}$ of Low-Side MOSFET
- Hiccup-Mode Under-Voltage Protection
- 118% Over-Voltage Protection
- Adjustable Output Voltage
- Small Converter Size
  - 300kHz Constant Switching Frequency
  - Small SOP-8 Package
- Built-In Digital Soft-Start
- Shutdown Control using an External MOSFET
- Lead Free Available (RoHS Compliant)

Applications

- Motherboard
- Graphics Card
- High Current, up to 20A, DC-DC Converters

General Description

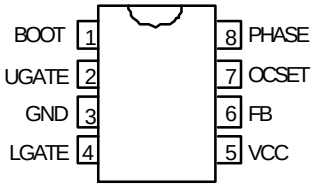
The APW7120 is a fixed 300kHz frequency, voltage mode, synchronous PWM controller. The device drives two low cost N-channel MOSFETs and is designed to work with single 5~12V or two supply voltage(s), providing excellent regulation for load transients.

The APW7120 integrates controls, monitoring and protection functions into a single 8-pin package to provide a low cost and perfect power solution.

A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. An internal 0.8V reference provides low output voltage down to 0.8V for further applications. An built-in digital soft-start with fixed soft-start interval prevents the output voltage from overshoot as well as limiting the input current. The controller's over-current protection monitors the output current by using the voltage drop across the low-side MOSFET's $R_{DS(ON)}$, eliminating the need of a current sensing resistor. Additional under voltage and over voltage protections monitor the voltage on FB pin for short-circuit and over-voltage protections. The over-current protection cycles the soft-start function until 4 over-current events are counted.

Pulling and holding the voltage on OCSET pin below 0.15V with an open drain device shuts down the controller.

Pinouts



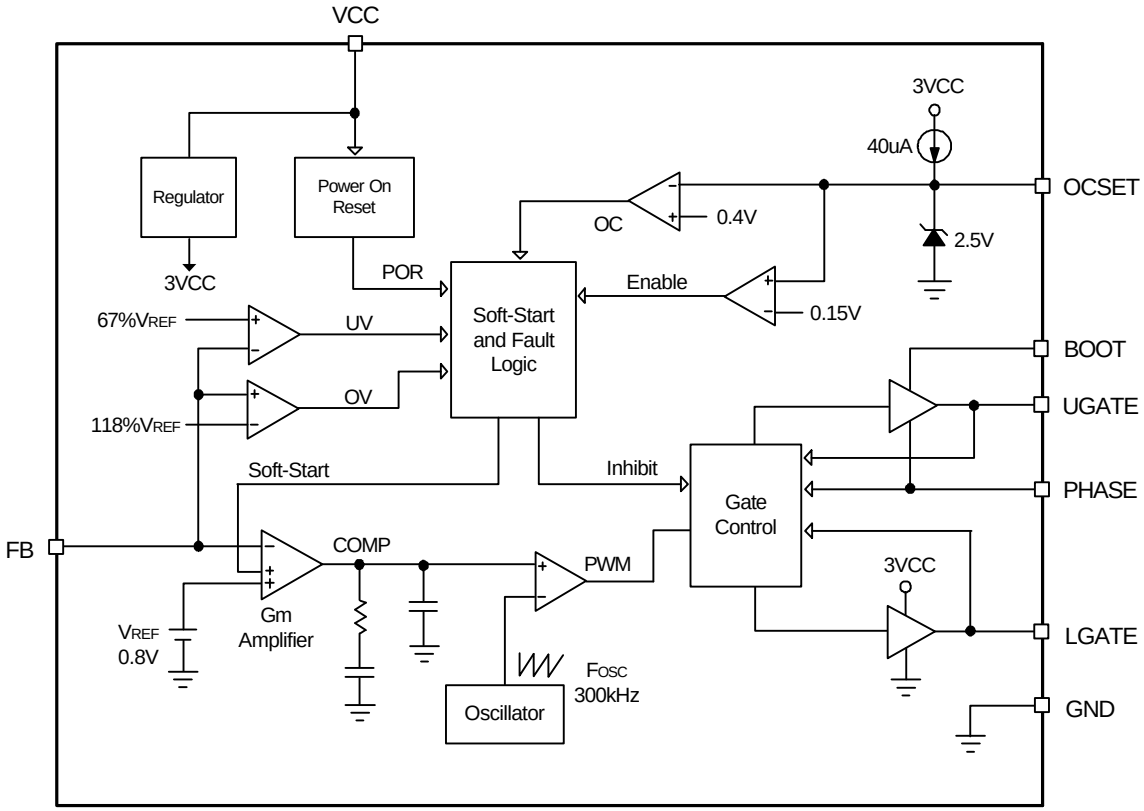
SOP-8

Ordering and Marking Information

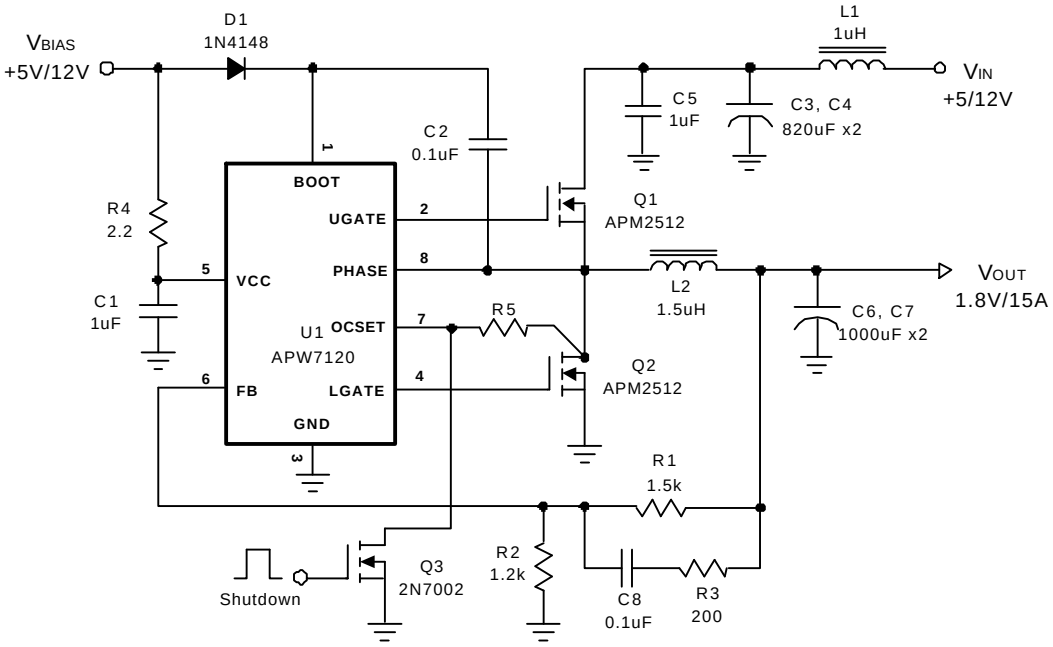
APW7120 □□-□□□ LeadFreeCode HandlingCode Temp.Range PackageCode	PackageCode K : SOP-8 Operating Ambient Temp. Range E : -20 to 70 °C HandlingCode TU : Tube TR : Tape & Reel LeadFreeCode L : Lead Free Device Blank : Original Device
APW7120 K : APW7120 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Application Circuit



C3, C4 : 820µF/16V , ESR=25 mΩ

C6, C7 : 1000µF/6.3V, ESR=30 mΩ

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 16	V
V_{BOOT}	BOOT Voltage (BOOT to PHASE)	-0.3 ~ 16	V
	UGATE Voltage (UGATE to PHASE) <400nS pulse width >400nS pulse width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <400nS pulse width >400nS pulse width	 -5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V
	PHASE Voltage (PHASE to GND) <400nS pulse width >400nS pulse width	 -10 ~ 30 -0.3 ~ 16	V
$V_{I/O}$	Input Voltage (OCSET, FB to GND)	-0.3 ~ 7	V
	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	300	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode) (Note 2)	±2	kV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 3)	160	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 13.2	V
V_{OUT}	Converter Output Voltage	0.8 ~ 80%V_{IN}	V
V_{IN}	Converter Input Voltage	2.2 ~ 13.2	V
I_{OUT}	Converter Output Current	0 ~ 20	A
T_A	Ambient Temperature	-20 ~ 70	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 4: Please refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC} = 12V, V_{BOOT} = 12V and T_A = -20 ~ 70°C. Typlcal values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7120			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VCC}	VCC Nominal Supply Current	UGATE and LGATE Open	-	2.1	6	mA
	VCC Shutdown Supply Current		-	1.5	4	mA
POWER-ON RESET						
	Rising VCC Threshold		3.8	4.1	4.4	V
	Hysteresis		0.3	0.45	0.6	V
OSCILLATOR						
F_{OSC}	Free Running Frequency		250	300	350	kHz
ΔV_{OSC}	Ramp Amplitude		-	1.5	-	V_{P-P}

Electrical Characteristics (Cont.)

Unless otherswise specified, these specifications apply over V_{CC} = 12V, V_{BOOT} = 12V and T_A = -20 ~ 70°C. Typlcal values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7120			Unit
			Min	Typ	Max	
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Measured at FB Pin	-	0.8	-	V
	Accuracy	T_A =-20~70°C	-2.0	-	+2.0	%
	Line Regulation	V_{CC}=12 ~ 5V	-	0.05	0.5	%
ERROR AMPLIFIER						
	DC Gain		-	86	-	dB
F_{P1}	First Pole Frequency		-	0.4	-	Hz
F_Z	Zero Frequency		-	0.4	-	kHz
F_{P2}	Second Pole Frequency		-	430	-	kHz
	Average UGATE Duty Range		0	-	85	%
	FB Input Current		-	-	0.1	µA
PWM CONTROLLER GATE DRIVERS						
	UGATE Source	$V_{BOOT-PHASE}$ =12V, $V_{UGATE-PHASE}$ =6V	1.0	2.0	-	A
	UGATE Sink	$V_{BOOT-PHASE}$ =12V, $V_{UGATE-PHASE}$=1V	-	3.5	7	Ω
	LGATE Source	V_{CC}=12V, V_{LGATE}=6V	1.0	1.9	-	A
	LGATE Sink	V_{CC}=12V, V_{LGATE}=1V	-	2.6	5	Ω
T_D	Dead-Time	Guaranteed by Design	-	40	100	nS
PROTECTIONS						
I_{OCSET}	OCSET Current Source	V_{PHASE}=0V, Normal Operation	35	40	45	µA
	Over-Current Reference Voltage	T_A =-20~70°C	0.37	0.4	0.43	V
U_{VFB}	FB Under-Voltage Threshold	Rising V_{FB}	64	67	70	%
	FB Under-Voltage Hysteresis		-	45	-	mV
	Over-Voltage Threshold	Rising V_{FB}	115	118	121	%
SOFT-START AND SHUTDOWN						
T_{SS}	Soft-Start Interval		2	3.8	5	mS
	OCSET Shutdown Threshold	Falling V_{OCSET}	0.1	0.15	0.3	V
	OCSET Shutdown Hysteresis		-	40	-	mV

Functional Pin Description

BOOT (Pin 1)

This pin provides ground referenced bias voltage to the high-side MOSFET driver. A bootstrap circuit with a diode connected to 5~12V is used to create a voltage suitable to drive a logic-level N-channel MOSFET.

UGATE (Pin 2)

Connect this pin to the high-side N-channel MOSFET's gate. This pin provides gate drive for the high-side MOSFET.

GND (Pin 3)

The GND terminal provides return path for the IC's bias current and the low-side MOSFET driver's pull-low current. Connect the pin to the system ground via very low impedance layout on PCBs.

LGATE (Pin 4)

Connect this pin to the low-side N-channel MOSFET's gate. This pin provides gate drive for the low-side MOSFET.

VCC (Pin 5)

Connect this pin to a 5~12V supply voltage. This pin provides bias supply for the control circuitry and the low-side MOSFET driver. The voltage at this pin is monitored for the Power-On Reset (POR) purpose.

FB (Pin 6)

This pin is the inverting input of the internal Gm amplifier. Connect this pin to the output (V_{OUT}) of the converter via an external resistor divider for closed-loop operation. The output voltage set by the resistor divider is determined using the following formula :

$$V_{OUT} = 0.8V \cdot (1 + \frac{R1}{R2}) \qquad (V)$$

where R1 is the resistor connected from V_{OUT} to FB , and R2 is the resistor connected from FB to GND. The FB pin is also monitored for under and over-voltage events.

OCSET (Pin 7)

The OCSET is a dual-function input pin for over-current protection and shutdown control. Connect a resistor (R_{OCSET}) from this pin to the Drain of the low-side MOSFET. This resistor, an internal 40μA current source (I_{OCSET}), and the MOSFET's on-resistance (R_{DSON}) set the converter over-current trip level (I_{PEAK}) according to the following formula:

$$I_{PEAK} = \frac{40\mu A \cdot R_{OCSET} - 0.4V}{R_{DSON}} \qquad (A)$$

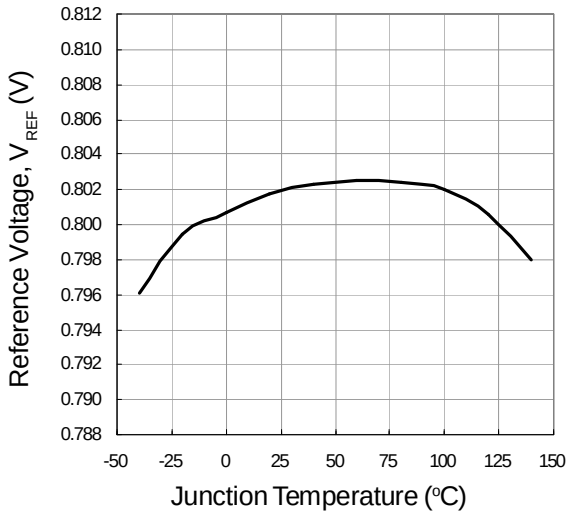
Pulling and holding this pin below 0.15V with an open drain device, with very low parasitic capacitor, shuts down the IC with floating output and also resets the over-current counter. Releasing OCSET pin initiates a new soft-start and the converter works again.

PHASE (Pin 8)

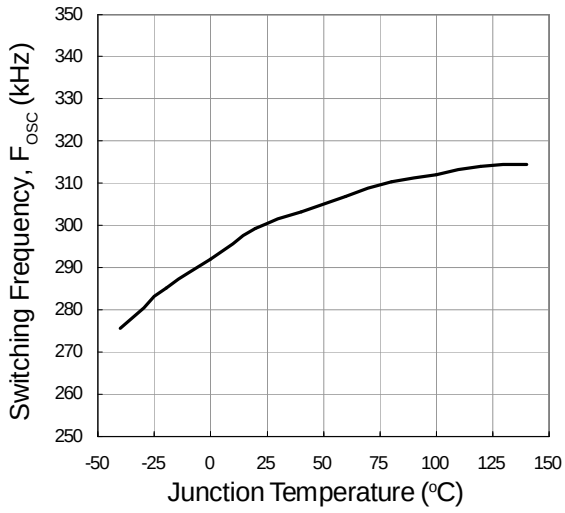
The pin provides return path for the high-side MOSFET driver's pull-low current. Connect this pin to the high-side MOSFET's source.

Typical Operating Characteristics

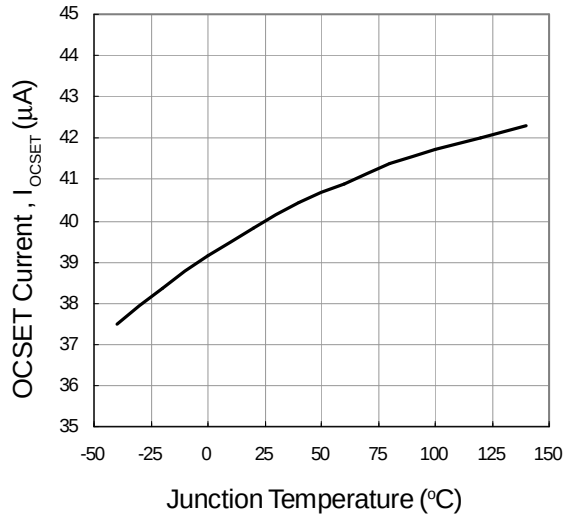
Reference Voltage vs Junction Temperature



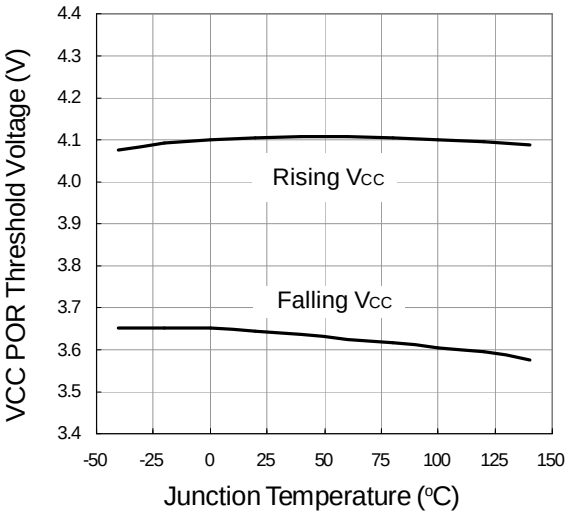
Switching Frequency vs Junction Temperature



OCSET Current vs Junction Temperature

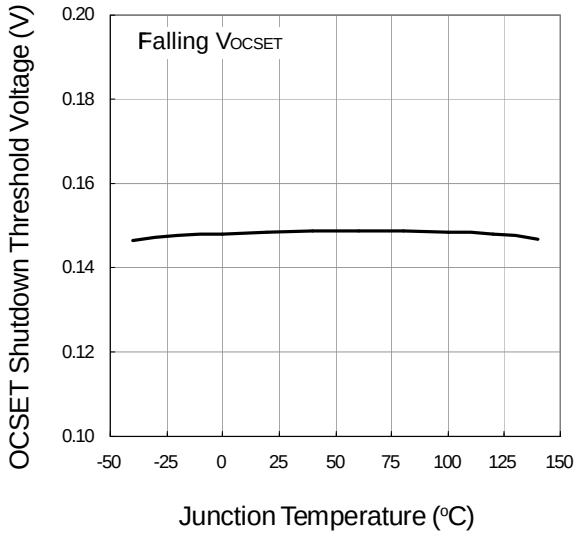


VCC POR Threshold Voltage vs Junction Temperature



Typical Operating Characteristics (Cont.)

OCSET Shutdown Threshold Voltage
vs Junction Temperature



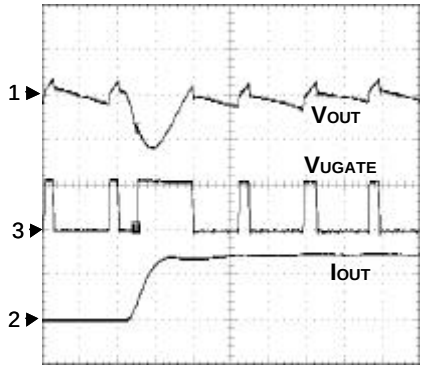
Operating Waveforms

(Refer to the typical application circuit, V_{BAIS}=V_{IN}=+12V supplied by an ATX Power Supply)

1. Load Transient Response : I_{OUT} = 0A -> 15A -> 0A

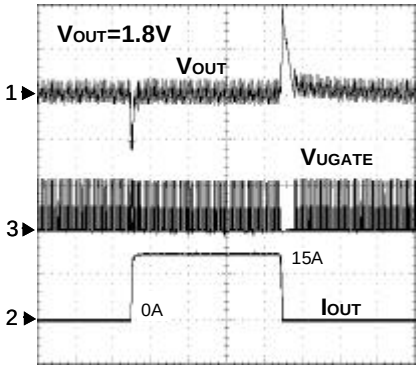
- I_{OUT} slew rate = ±15A/μS

I_{OUT} = 0A -> 15A



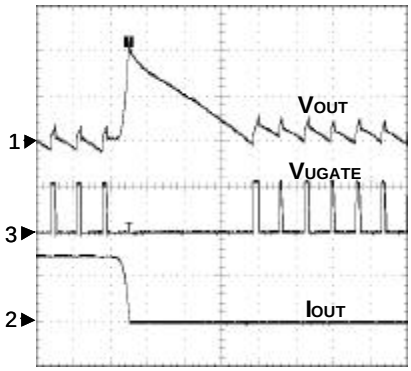
Ch1 : VOUT, 100mV/Div, DC, Offset = 1.8V
Ch2 : IOUT, 10A/Div
Ch3 : VUGATE, 20V/Div, DC
Time : 2μS/Div
BW = 20 MHz

I_{OUT} = 0A -> 15A -> 0A



Ch1 : VOUT, 100mV/Div, DC, Offset = 1.8V
Ch2 : IOUT, 10A/Div
Ch3 : VUGATE, 20V/Div, DC
Time : 50μS/Div
BW = 20 MHz

I_{OUT} = 15A -> 0A



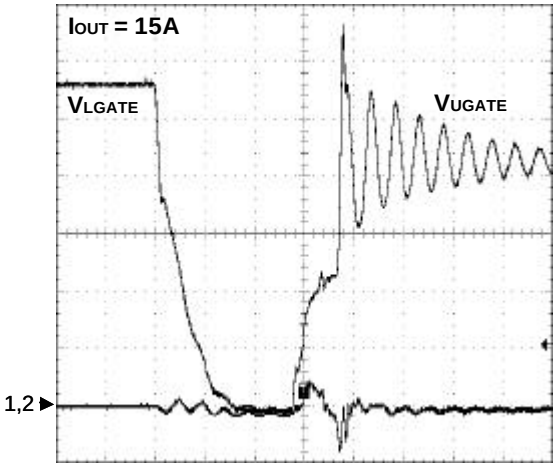
Ch1 : VOUT, 100mV/Div, DC, Offset = 1.8V
Ch2 : IOUT, 10A/Div
Ch3 : VUGATE, 20V/Div, DC
Time : 2μS/Div
BW = 20 MHz

Operating Waveforms (Cont.)

(Refer to the typical application circuit, V_{BIAS}=V_{IN}=+12V supplied by an ATX Power Supply)

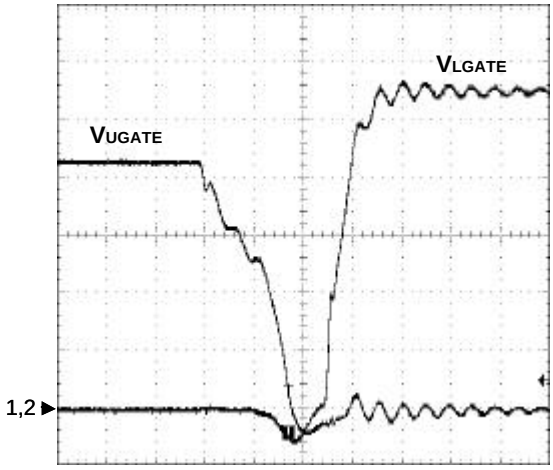
2. UGATE and LGATE Switching Waveforms

Rising V_{UGATE}



Ch1 : VUGATE, 5V/Div, DC
Ch2 : VLGATE, 2V/Div, DC
Time : 20nS/Div
BW = 500 MHz

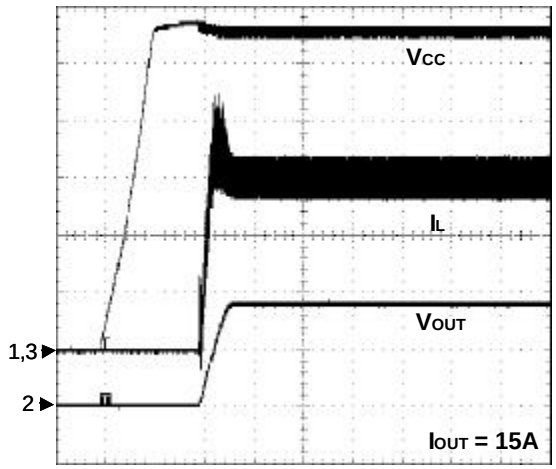
Falling V_{UGATE}



Ch1 : VUGATE, 5V/Div, DC
Ch2 : VLGATE, 2V/Div, DC
Time : 20nS/Div
BW = 500 MHz

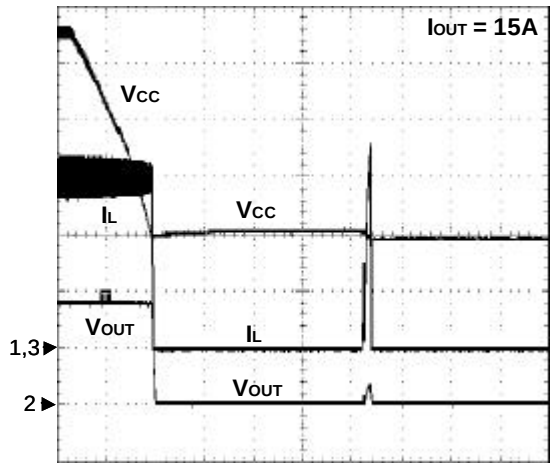
3. Powering ON / OFF

Powering ON



Ch1 : VCC, 2V/Div, DC
Ch2 : VOUT, 1V/Div, DC
Ch3 : IL, 5A/Div, DC
Time : 5mS/Div
BW = 20 MHz

Powering OFF



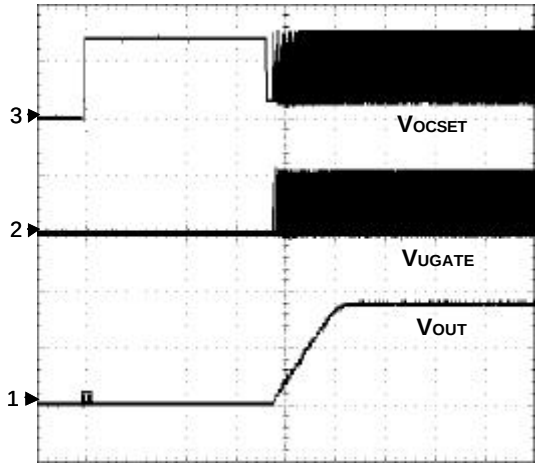
Ch1 : VCC, 2V/Div, DC
Ch2 : VOUT, 1V/Div, DC
Ch3 : IL, 5A/Div, DC
Time : 5mS/Div
BW = 20 MHz

Operating Waveforms (Cont.)

(Refer to the typical application circuit, V_{BIAS}=V_{IN}=+12V supplied by an ATX Power Supply)

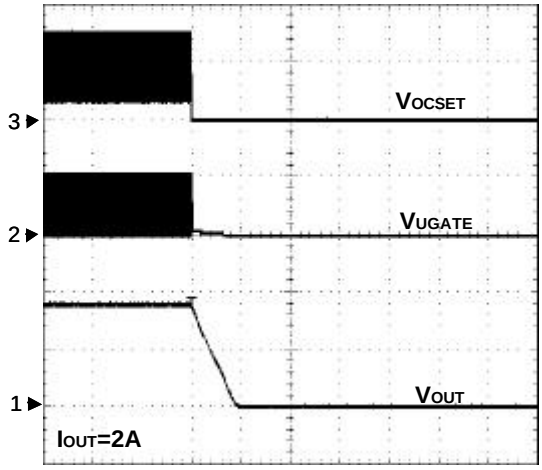
4. Enabling and Shutting Down

Enabling by Releasing OCSET Pin



Ch1 : VOUT, 1V/Div, DC Ch2 : VUGATE, 20V/Div, DC
Ch3 : VOCSET, 2V/Div, DC Time : 2mS/Div
BW = 20 MHz

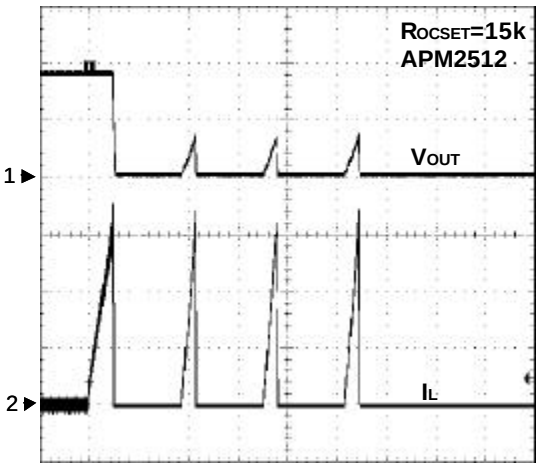
Shutting Down by Pulling OCSET Low



Ch1 : VOUT, 1V/Div, DC Ch2 : VUGATE, 20V/Div, DC
Ch3 : VOCSET, 2V/Div, DC Time : 2mS/Div
BW = 20 MHz

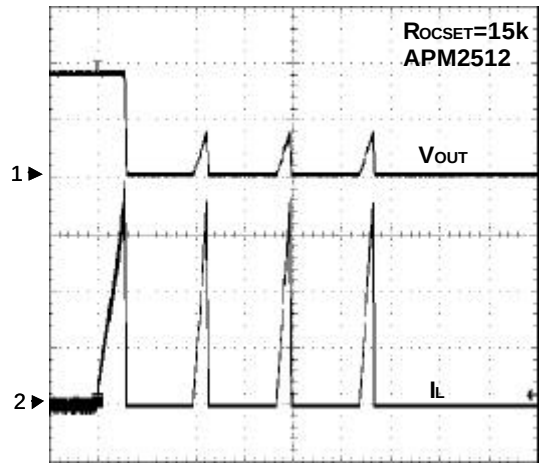
5. Over-Current Protection

No Connecting a shutdown MOSFET at OCSET Pin



Ch1 : VOUT, 1V/Div, DC Ch2 : IL, 10A/Div, DC
Time : 5mS/Div BW = 20 MHz

Connecting a shutdown MOSFET (2N7002) at OCSET Pin



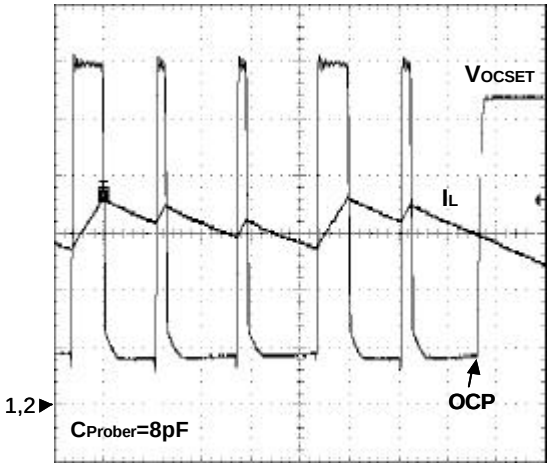
Ch1 : VOUT, 1V/Div, DC Ch2 : IL, 10A/Div, DC
Time : 5mS/Div BW = 20 MHz

Operating Waveforms (Cont.)

(Refer to the typical application circuit, V_{BIAS}=V_{IN}=+12V supplied by an ATX Power Supply)

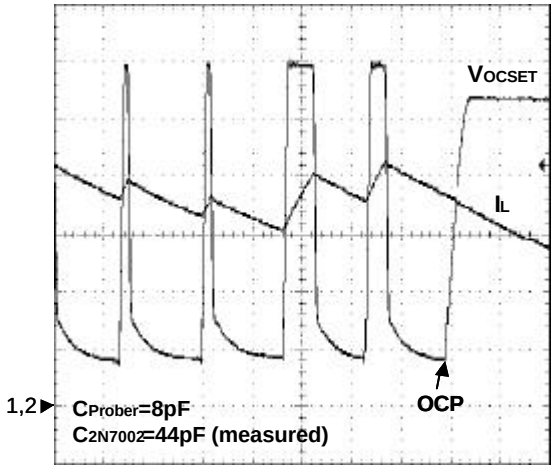
6. OCSET Voltage RC Delay

No Connecting a shutdown MOSFET at OCSET Pin



Ch1 : V_{OCSET}, 0.5V/Div, DC Ch2 : I_L, 10A/Div, DC
Time : 2μS/Div BW = 20 MHz

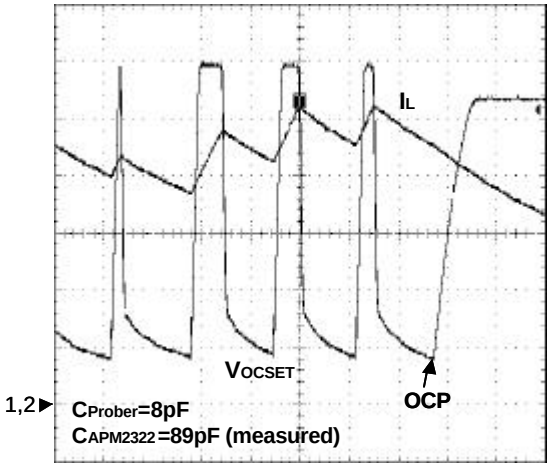
Connecting a shutdown MOSFET (2N7002) at OCSET Pin



Ch1 : V_{OCSET}, 0.5V/Div, DC Ch2 : I_L, 10A/Div, DC
Time : 2μ S/Div BW = 20 MHz

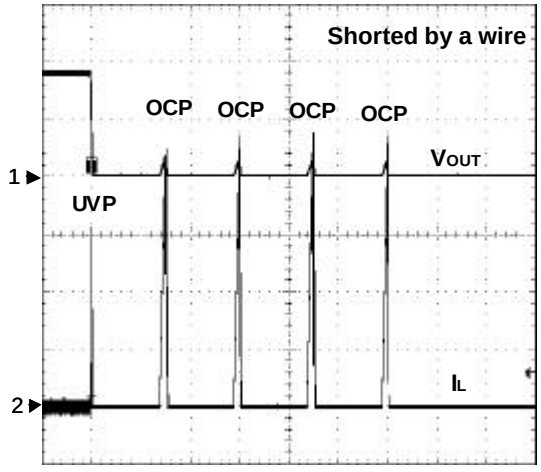
6. OCSET Voltage RC Delay (Cont.)

Connecting a shutdown MOSFET (APM2322) at OCSET Pin



Ch1 : V_{OCSET}, 0.5V/Div, DC Ch2 : I_L, 10A/Div, DC
Time : 2μS/Div BW = 20 MHz

7. Short-Circuit Test



Ch1 : V_{OUT}, 1V/Div, DC Ch2 : I_L, 10A/Div, DC
Time : 5mS/Div BW = 20 MHz

Functional Description

Power-On-Reset (POR)

The APW7120 monitors the VCC voltage (V_{CC}) for Power-On-Reset function, preventing wrong logic operation during powering on. When the VCC voltage is ready, the APW7120 starts a start-up process and then ramps the output voltage up to the target voltage.

Soft-Start

The APW7120 has a built-in digital soft-start to control the output voltage rise and limit the current surge at the start-up. During soft-start, an internal ramp connected to the one of the positive inputs of the Gm amplifier rises up from 0V to 2V to replace the reference voltage (0.8V) until the ramp voltage reaches the reference voltage. The soft-start interval is about 3.2ms typical, independent of the converter's input and output voltages.

Over-Current Protection(OCP)

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage, product of the inductor's current and the on-resistance, of the low-side MOSFET during it's on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

A resistor (R_{OCSET}), connected from the OCSET to the low-side MOSFET's drain, programs the over-current trip level. An internal 40μA (typical) current source flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET}. When the V_{OCSET} (V_{ROCSET}+ V_{DS} of the low-side MOSFET) is less than the internal over-current reference voltage (0.4V, typical), the IC shuts off the converter and then initiates a new soft-start process. After 4 over-current events are counted, the device turns off both high-side and low-side MOSFETs and the converter's output is latched to be floating.

Please pay attention to the RC delay effect. It causes the OCP trip level to be the function of the operating duty. The parasitic capacitance (including the capacitance inside the OCSET, external PCB trace capacitance and the C_{OSS} of the shutdown MOSFET) must be minimized, especially selecting a shutdown MOSFET with very small C_{OSS}. The OCP trip level follows the duty to increase a little at low operating duty, but very much at high operating duty, like the RC delay curve. Due to load regulation or current-limit, heavy load normally reduces converter's input voltage and increases the power loses. During heavy load, the APW7120 regulates the output voltage by expending the duty. This rises up the OCP trip level at the same time.

Under-Voltage Protection (UVP)

The under-voltage function monitors the FB voltage (V_{FB}) to protect the converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (67% V_{REF}), the APW7120 shuts off the converter. After a preceding delay, which starts at the beginning of the under-voltage shutdown, the APW7120 initiates a new soft-start to resume regulating. The under-voltage protection shuts off and then re-starts the converter repeatedly without latching. The function is disabled during soft-start process.

Over-Voltage Protection (OVP)

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage. When the output voltage rises to 118% of the nominal output voltage, the APW7120 turns on the low-side MOSFET until the output voltage falls below the OVP threshold, regulating the output voltage around the OVP thresholds.

Functional Description (Cont.)

Adaptive Shoot-Through Protection

The gate driver incorporates adaptive shoot-through protection to high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the low-side MOSFET, the LGATE voltage is monitored until it reaches a 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE-to-PHASE voltage is also monitored until it reaches a 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Shutdown Control

Pulling the OCSET voltage below 0.15V by an open drain transistor, shown in typical application circuit, shuts down the APW7120 PWM controller. In shut-down mode, the UGATE and LGATE are pulled to PHASE and GND respectively, the output is floating.

Application Information

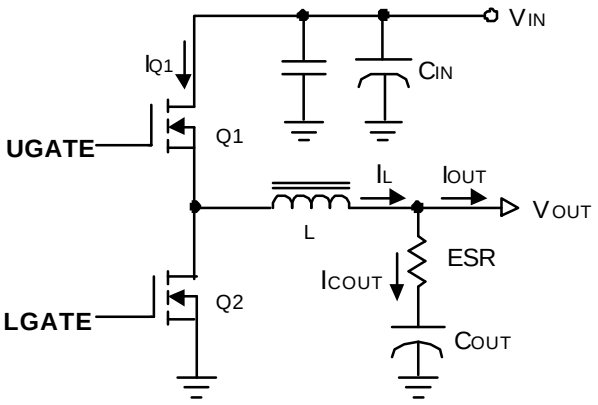
Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET(Q1) turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of low-side MOSFET(Q2).

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current of the bulk input capacitor is calculated as the following equation :

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \qquad (A)$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.



Application Information (Cont.)

Input Capacitor Selection (Cont.)

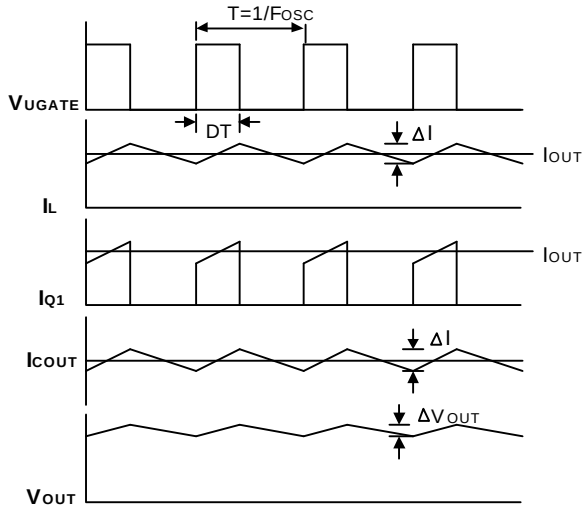


Figure 1 Buck Converter Waveforms

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calculated as the following equations :

$$V_{OUT} = D \cdot V_{IN} \quad (V) \ldots\ldots\ldots (1)$$

$$\Delta I = \frac{V_{OUT} \cdot (1 - D)}{F_{OSC} \cdot L} \quad (A) \ldots\ldots\ldots (2)$$

$$V_{ESR} = \Delta I \cdot ESR \quad (V) \ldots\ldots\ldots (3)$$

The peak-to-peak voltage of the ideal output capacitor is calculated as the following equations :

$$\Delta V_{COUT} = \frac{\Delta I}{8 \cdot F_{OSC} \cdot C_{OUT}} \quad (V) \ldots\ldots (4)$$

For general applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore the AC peak-to-peak output voltage is shown below:

$$\Delta V_{OUT} = \Delta I \cdot ESR \quad (V) \ldots\ldots\ldots (5)$$

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.

An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage, see equations (2) and (5). Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance

Application Information (Cont.)

Output Inductor Selection (Cont.)

values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the APW7120 will provide either 0% or 85% (Average) duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for theapplication of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \cdot I_{TRAN}}{V_{IN} - V_{OUT}} \quad , \quad t_{FALL} = \frac{L \cdot I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the transient load current. These requirements are minimum and maximum output levels for the worst case response time.

MOSFET Selection

The APW7120 requires two N-Channel power MOSFETs. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components, conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the high-side and the low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses, since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the low-side MOSFET's body diode. The gate-charge losses are dissipated by the APW7120 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the high-side MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{High\ -\ Side} = I_{OUT}^2 \cdot R_{DSON} \cdot D + \frac{1}{2} \cdot I_{OUT} \cdot V_{IN} \cdot t_{SW} \cdot F_{OSC}$$

$$P_{Low\ -\ Side} = I_{OUT}^2 \cdot R_{DSON} \cdot (1 - D)$$

Where : t_{SW} is the switching interval

Layout Considerations

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator.

In general, interconnecting impedances should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and

Application Information (Cont.)

Layout Considerations (Cont.)

finally combined using ground plane construction or single point grounding. Figure 2 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Begin the layout by placing the power components first. Orient the power circuitry to chieve a clean power flow path. If possible make all the connections on one side of the PCB with wide, copper filled areas.

2. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.

3. The VCC decoupling capacitor should be right next to the VCC and GND pins. Capacitor C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.

4. Minimize the length and increase the width of the trace between UGATE/LGATE and the gates of the MOSFETs to reduce the impedance driving the MOSFETs.

5. Use an dedicated trace to connect the R_{OCSET} and the Drain pad of the low-side MOSFET, Kevin connection , for accurate current sensing.

6. Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore keep traces to these nodes as short as possible.

7. Place the decoupling ceramic capacitor C_{HF} near the Drain of the high-side MOSFET as close as possible. The bulk capacitors C_{IN} are also placed near the Drain.

8. Place the Source of the high-side MOSFET and the Drain of the low-side MOSFET as close possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

9. Use a wide power ground plane, with low impedance, to connects the C_{HF}, C_{IN}, C_{OUT}, Schottky diode and the Source of the low-side MOSFET to provide a low impedance path between the components for large and high frequency switching currents.

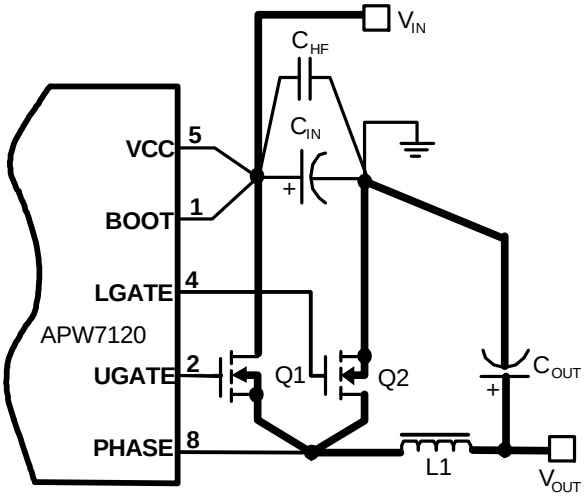
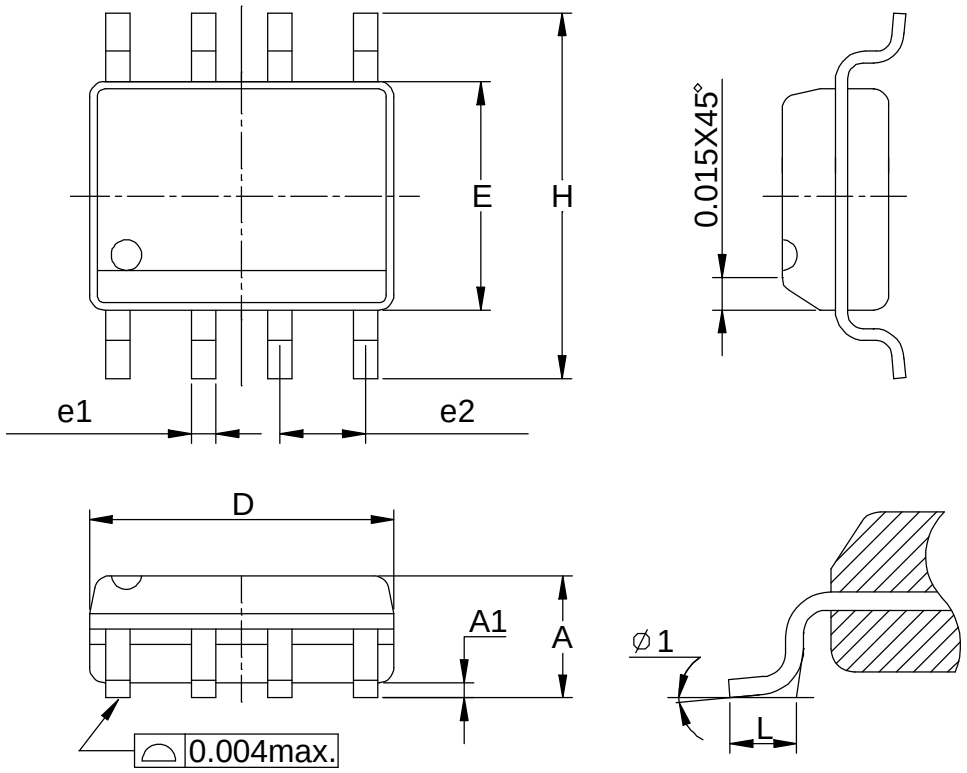


Figure 2 Recommended Layout Diagram

Package Information

SOP-8 pin (Reference JEDEC Registration MS-012)

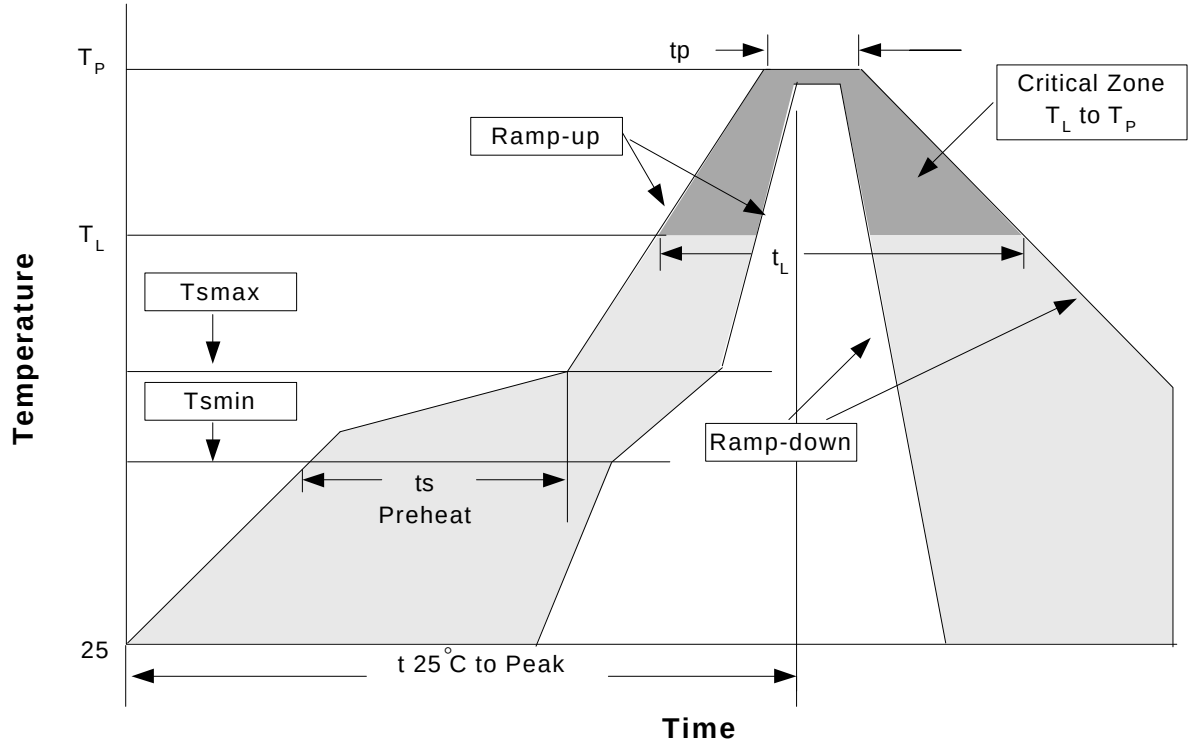


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

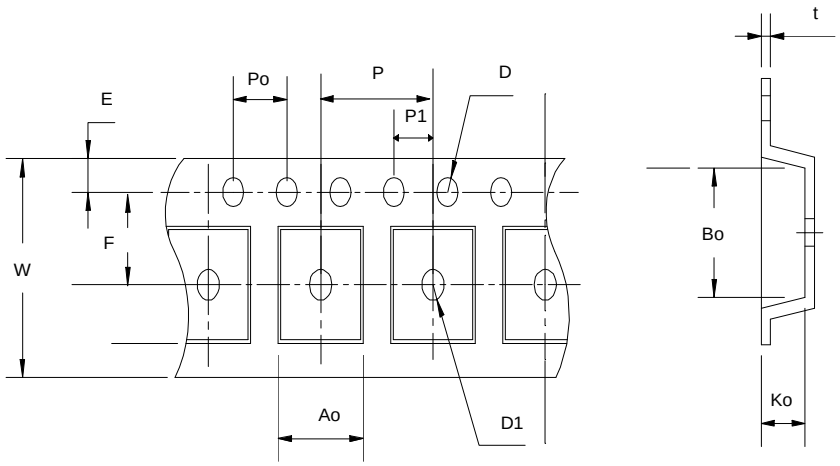
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

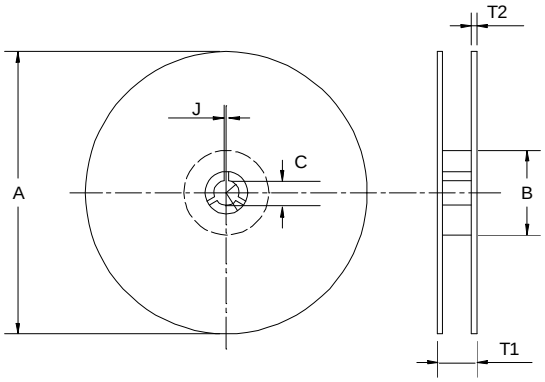
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions (Cont.)



Reel Dimensions

Application	A	B	C	J	T1	T2	W	P	E
SOP- 8	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500

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