

M62301SP,FP

10~12-BIT 4CH INTEGRATING A-D CONVERTER

DESCRIPTION

M62301 semiconductor integrated circuit forms an integrating A-D converter, being connected to a microcomputer unit. By using selection signals and counter clock signals from the unit, a 10~12-bit A-D converter can be created at a low cost.

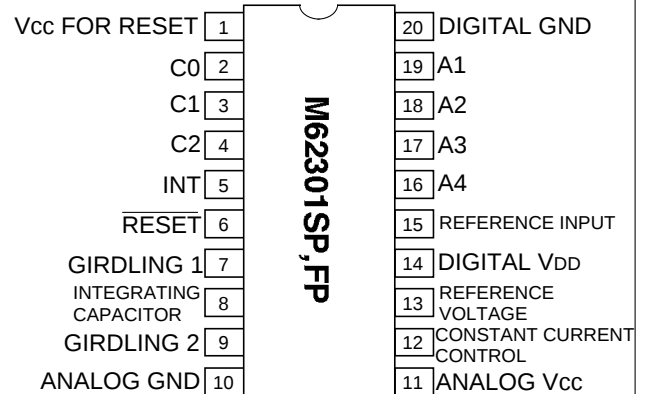
The integration time and resolution can be set at the user's option by changing external parameters. In addition, the built-in circuit offset, delay time and temperature fluctuation are adjustable, enabling a wide range of applications.

M62301 has a 3 input decoder circuit, high-precision reference voltage (1.22V) generator, current supply and comparator for integration, and voltage-monitoring reset circuit for a 5V power supply. It is also equipped with girdling to prevent current leak from integration capacitor.

FEATURES

- Separate power supplies for analog section and digital section.
- Low power dissipation.....2mA(typ)
(1mA for A-D conversion and the other 1mA for reset)
- Linear error..... $\pm 0.02\%$ (typ)
- Conversion time.....526 μ s/ch(typ)
- Built-in system reset.....4.45V(typ)

PIN CONFIGURATION (TOP VIEW)

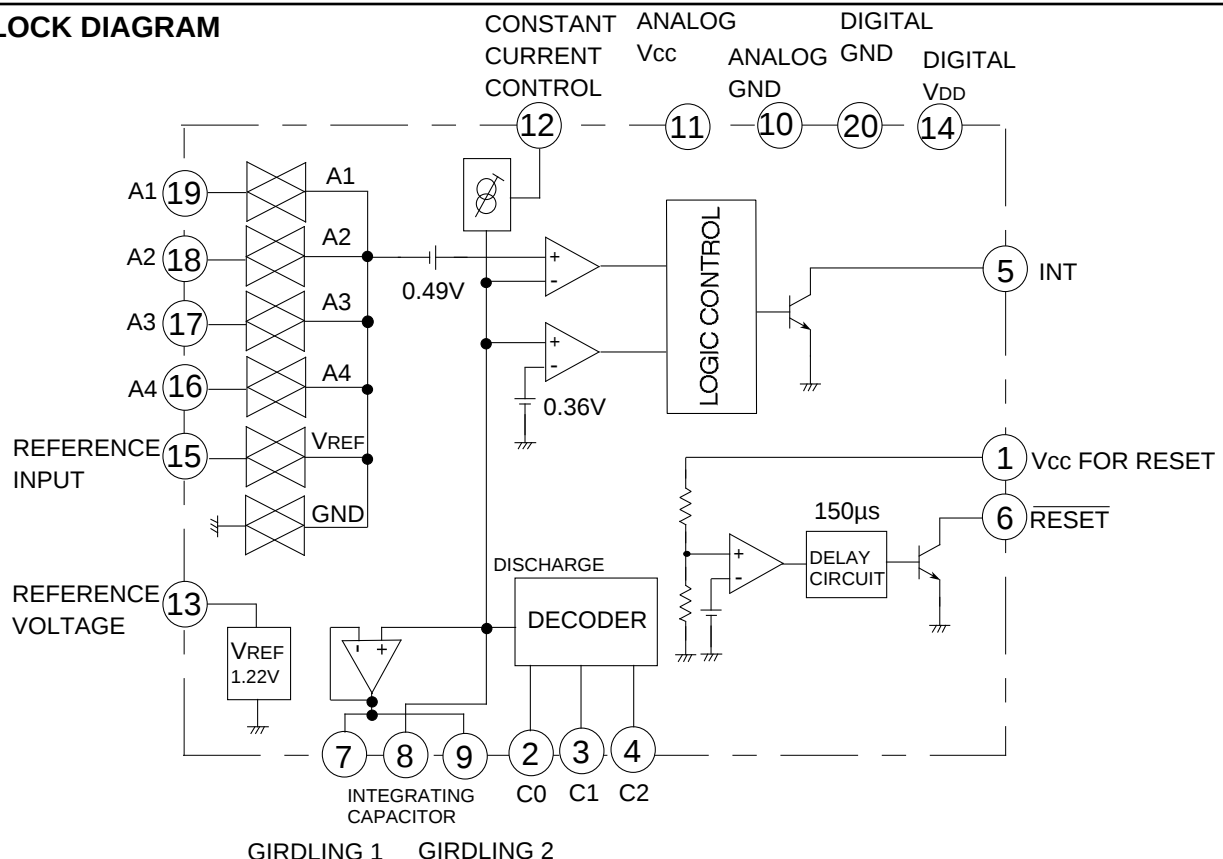


Outline 20P4B(SP)
20P2N-A(FP)

APPLICATION

High-precision control systems such as temperature control and speed control

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Analog section supply voltage		15	V
V _{DD}	Digital section supply voltage		8	V
V _{ID}	Digital input voltage		-0.3~V _{DD} +0.3	V
V _{IA}	Analog input voltage		-0.3~V _{DD} +0.3	V
I _{OINT}	INT output current		6	mA
I _{ORE}	Reset output current		6	mA
V _{INT}	INT output withstand voltage		15	V
V _{RESET}	Reset output withstand voltage		15	V
V _{RE}	Reset supply voltage		6	V
P _d	Power dissipation		990(DIP)/660(FP)	mW
K _θ	Thermal derating		9.9(DIP)/6.6(FP)	mW/°C
T _{opr}	Operating temperature		-20 ~ +75	°C
T _{stg}	Storage temperature		-55 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Analog section supply voltage	4.5	8.0	12.0	V
V _{DD}	Digital section supply voltage	4.5	5.0	5.5	V
V _{IA}	Analog input voltage range (I _I =50μA)	0		No more than(V _{CC} -2.5V) and V _{DD} (Note 1)	V
V _{IR}	Reference input voltage(I _I =50μA)	1	—	No more than(V _{CC} -2.5V) and V _{DD} (Note 1)	V
C _I	Integration capacity	300	—	22000	pF
R _I	Resistance to determine charge current	6	—	60	kW
I _O	Output current		—	4	mA

Note 1.Maximum analog input voltage is less than the difference between V_{CC}-2.5V as well as V_{DD}.

*Charging current I_I= $\frac{V_{REF}}{R1}$

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ELECTRICAL CHARACTERISTICS(V_{CC}=5.0V,V_{DD}=5.0V,T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
A-D converter	I _{CC}	Supply current	—	1.0	2.0	mA
	V _{IA}	Analog input voltage range	0		2.5	V
					2.2	
	V _{REF}	Reference input voltage	1.17	1.22	1.27	V
	I _{REF} ⊕	Permissible current inflow at reference voltage			50	μA
	I _{REF} ⊖				-10	
	E _C	Conversion error	(Note 1)R _I =24kΩ	0.05	0.1	%/FSR
	E _L	Linear error	(Note 2)R _I =24kΩ	0.02	0.09	%/FSR
	T _T	Conversion time	V _{IA} =2.5V,C _I =0.01μF R _I =24kΩ	526		μs
	T _{di}	Discharge time	V 8=3V→0.3V C _I =4700pF	3	17	μs
	I _B	Analog input current		-0.35	-3.5	μA
	V _{IH}	Digital input "H" level	3.5			V
	V _{IL}	Digital input "L" level			0.8	V
	V _{LINT}	INT output "L" level	I _{OL} =1mA	0.1	0.4	V
Reset section	I _{OHINT}	INT output leak current	V 5=15V	—	1	μA
	V _{DET}	Detection voltage	4.30	4.45	4.60	V
	DV _{DET}	Hysteresis voltage	30	50	80	mV
	T _{DE}	Delay time	75	150	300	μs
	V _{LRE}	Reset output "L" level	I _{OL} =1mA	0.1	0.4	V
	I _{OHRE}	Reset output leak current	V 5=15V	—	1	μA
	I _{RE}	Supply current	V _{RE} =5V	1.0	2.0	mA
	V _{OPL}	Limit operating voltage	R _L =2.2kΩ,V _{LRE} ±0.4V R _L =100kΩ,V _{LRE} ±0.4V	0.75 0.6	1.0 0.8	V

Note 1.Conversion error;Deviation from the line that links the "0" scale point (mode 0) and reference scale point (mode 3. V_{FSR}=2.5V).Associated with all channels.

Note 2.Linear error;Deviation from the line that links the 0-V input point and 2.5V input point on a given channel.

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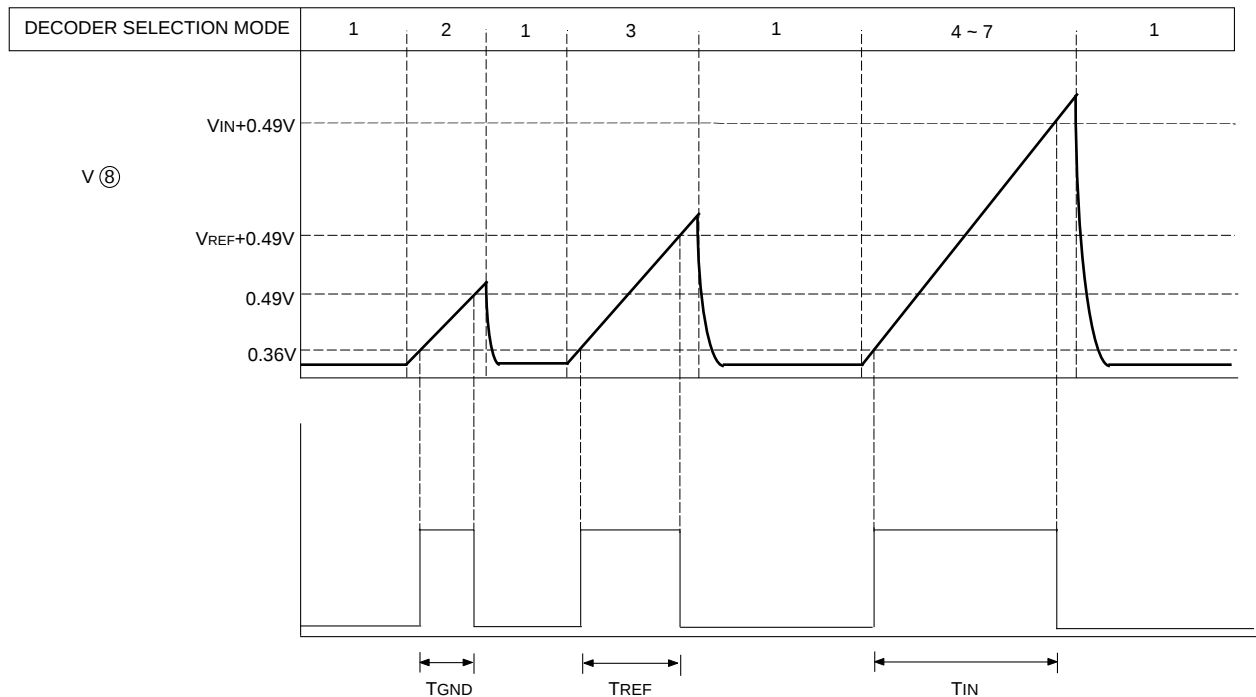
OPERATING DESCRIPTION

(1)Decoder

Based on digital inputs to C0,C1,C2,the analog switch is set to on,and the input of "0" scale (GND input),input of reference scale (reference voltage input),input to A1~A4,or discharge from integration capacitor (C_i) is performed.None of these operations is performed when the "mode 8" input is given:

Mode	1	2	3	4	5	6	7	8
C0	0	1	0	1	0	1	0	1
C1	0	0	1	1	0	0	1	1
C2	0	0	0	0	1	1	1	1
	Discharge	GND	VREF	A1	A2	A3	A4	—

(2)A-D conversion



Multiplexer first selects V_{GND},obtaining minimum pulse T_{GND}.It then selects V_{REF},obtaining reference pulse T_{REF}.Input is selected next,obtaining input pulse T_{IN}.V_{IN} is obtained by deducting T_{GND},as the offset,from T_{REF} and T_{IN}.

$$V_{IN}=V_{REF} \cdot \frac{T_{IN}-T_{G}}{T_{REF}-T_{G}}$$

By measuring voltage at the maximum input for approximately 500μs under the counter clock of 8MHz,resolution of approximately 12bits can be obtained;

$$\frac{500\mu s}{125ns} \approx 2^{12}$$

Note. To ensure discharge from capacitor C_i,the decoder input as in

the above diagram should stay in mode 1 at least for the

$$\text{period calculated above: } T_{di}=(C_i \times \frac{V_{I\max}+0.49}{1mA})$$

It is not necessary to measure T_{GND},and T_{REF} for each

channel.

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(3)Constant current control

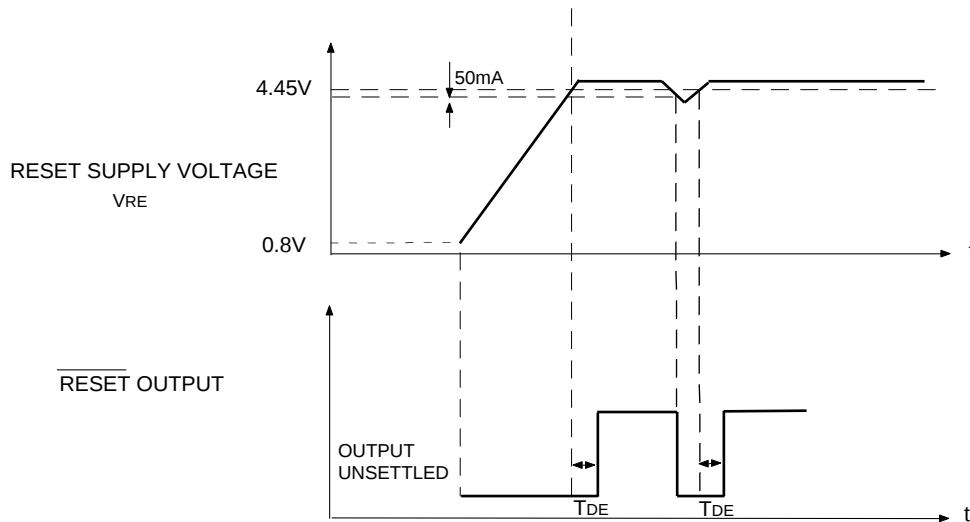
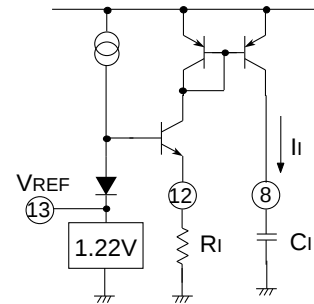
Integrating current I_i can be obtained based on the reference voltage(1.22V)by the built-in high-precision generator and resistance R_i .

$$I_i = \frac{1.22}{R_i} \text{ (A)} \dots\dots\dots(1)$$

Integration time T_i can be calculated as follows;

$$T_i = (V_{IN} + 0.49) \frac{C_i}{I_i} \dots\dots\dots(2)$$

(However,parameters such as built-in comparator offset voltage,analog switch offset,voltage leak current and delay time are not counted.)



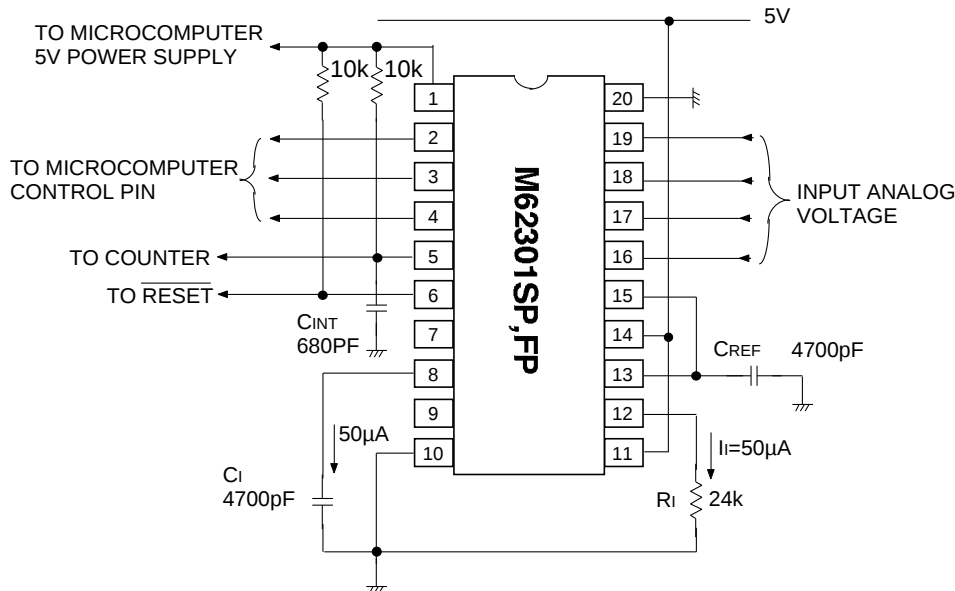
When voltage applied to pin V_{RE} becomes less than 4.45V,the RESET output status becomes "L".If voltage increases over 4.50V,the RESET status becomes "H" within 150μsec.

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APPLICATION SUGGESTION

1.4-channel 11-bit A-D converter system



CREF: To stabilize reference voltage, be sure to connect capacitance of approximately 4700pF.

CINT: We suggest that this capacitance be connected to prevent malfunction due to noise.

Use Ci that leaks as slight current as possible. To prevent leak to the circuit board, we recommend providing girdling ⑦, ⑨

$$\text{Charge current } I_i = \frac{1.22\text{V}}{24\text{k}\Omega} \approx 50\mu\text{A}$$

Resolution depends on the number of microcomputer counter clock pulses that are generated while the INT output status is "high" at the maximum input voltage 2.5V (VCC-2.5V).

When the microcomputer counter clock frequency is 8MHz, the resolution can be calculated by using the constant calculated above, as follows;

$$\frac{4700\text{pF} \times \frac{(2.5+0.13)}{50\mu\text{A}}}{\frac{1}{8\text{M}}} \approx 2^{11}$$

Therefore, the resolution of this system is approximately 11 bits.

2.4-channel 12-bit A-D converter system

[illegible]

Use CI that leaks as slight current as possible. To prevent leak to the circuit board, we recommend providing girdling ⑦, ⑨.

$$\frac{6800\text{pF} \times \frac{(5 + 0.13)}{50\mu\text{A}}}{\frac{1}{8\text{M}}} \doteq 2^{12}$$

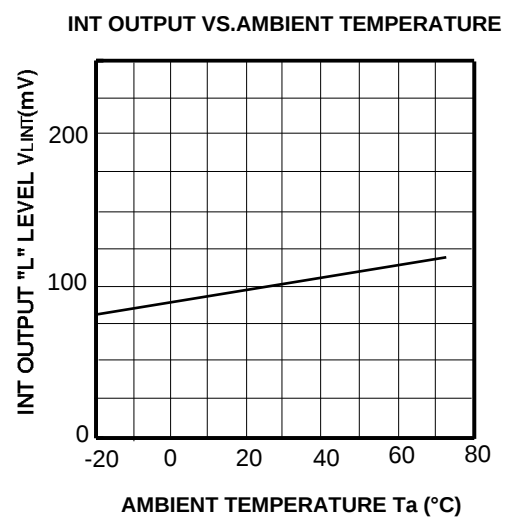
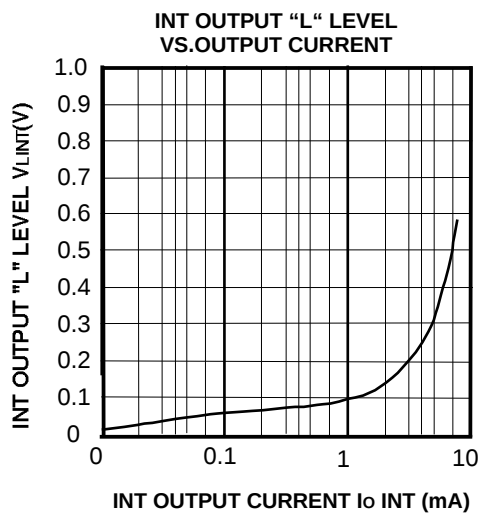
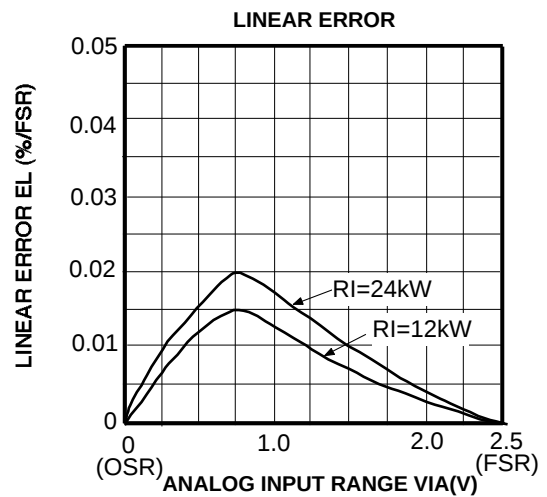
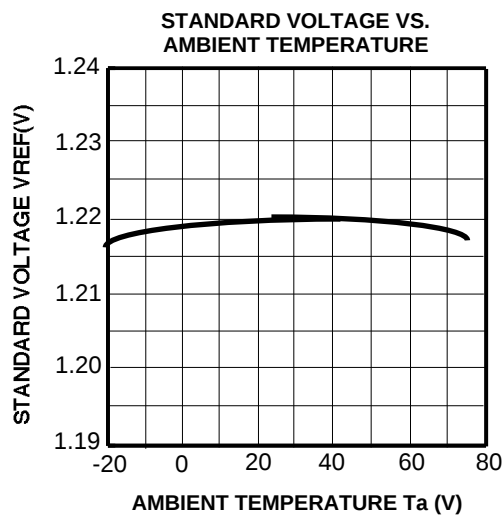
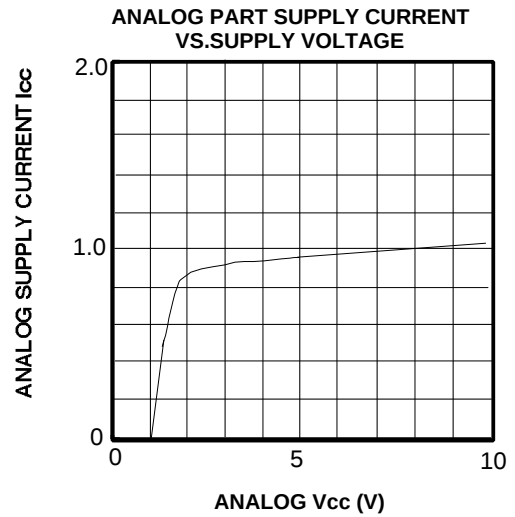
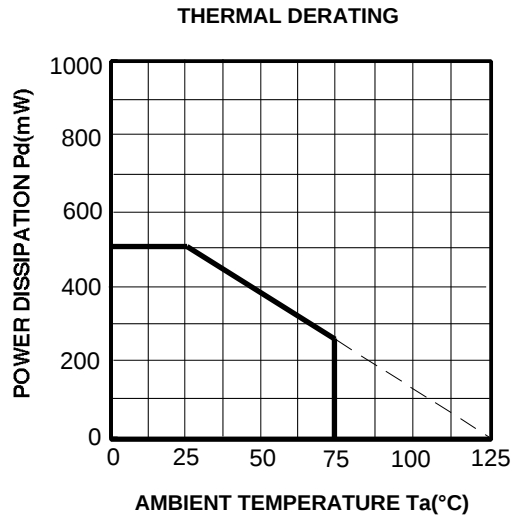
Counter clock	Resolution	Change current I _i (μA)	Resistance to determine constant current R _i (kW)	Integration capacitance C _i	Discharge time T _{di} (μs)
8MHz	10-bit	50	24	1400pF	7.7
		100	12	2800pF	15.4
	11-bit	50	24	2800pF	15.4
		100	12	5600pF	30.7
	12-bit	50	24	5600pF	30.7
		100	12	12000pF	65.9
16MHz	10-bit	50	24	700pF	3.9
		100	12	1400pF	7.7
	11-bit	50	24	1400pF	7.7
		100	12	2800pF	15.4
	12-bit	50	24	2800pF	15.4
		100	12	5600pF	30.7

The values in this table apply when $V_{I\text{Amax}}$ is 5V.

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TYPICAL CHARACTERISTICS



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